Victory Device

3D Device Simulation

Overview

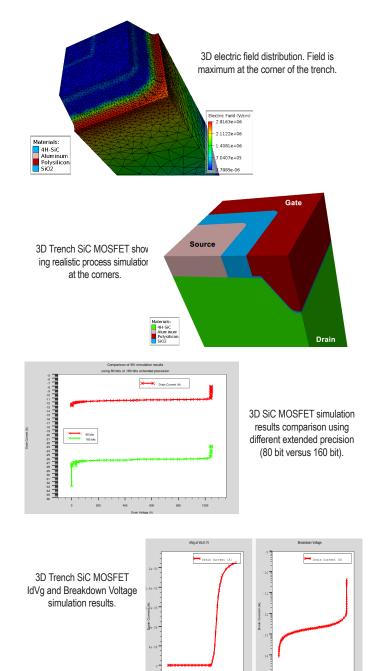
Victory Device is a general purpose 3D device simulator. A tetrahedral meshing engine is used for fast and accurate simulation of complex 3D geometries. Victory Device performs DC, AC, and transient analysis for silicon, binary, ternary, and quaternary material-based devices.

Features

- Tetrahedral mesh for accurate 3D geometry representation
- · Voronoi discretization for conformal Delaunay meshes
- Advanced physical models with user-customizable material database for silicon and compound materials
- · Stress-dependent mobility and bandgap models
- Customizable physical models using the C-Interpreter or dynamically linked libraries
- DC, AC, and transient analysis
- · Drift-diffusion and energy balance transport equations
- Self-consistent simulation of self-heating effects including heat generation, heat flow, lattice heating, heat sinks, and temperature-dependent material parameters
- Methods to simulate the electrochemical reaction and transport of an arbitrary number of chemical species
- Highly customizable chemistry models for simulation of performance degradation, atomic species transport, and complex charge-capture mechanisms
- · Advanced multi-threaded numerical solver library
- Atlas-compatible
- Silvaco's strong encryption is available to protect valuable customer and third party intellectual property

SiC Application Example

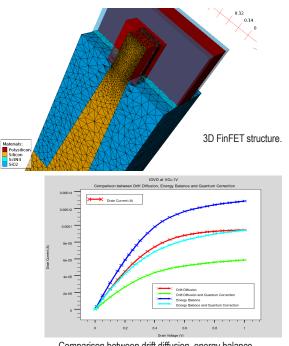
This 3D trench SiC MOSFET simulation includes rounded corners at the top and bottom of the trench. Automatic full 3D Delaunay mesh, corresponding discretization and extended precision numerics allow optimization of simulation time and accuracy.



0 4 8 12 16 Gate Votage (V) 0 100 200 310 400 500 610 700 800 Drain Votage (V)

FinFET Application Example

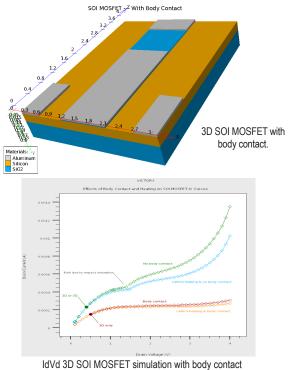
This 3D FinFET is simulated with a 3D fully unstructured tetrahedral mesh. The mesh is fully automated including refinement on doping and interfaces.



Comparison between drift diffusion, energy balance and quantum correction.

SOI Application Example

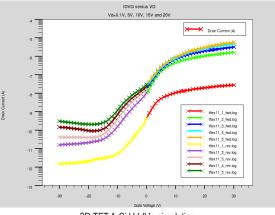
This 3D SOI MOSFET device simulation shows how to use a body contact to suppress the kink effect. Also shown is the effect of lattice heating on the IV curves.



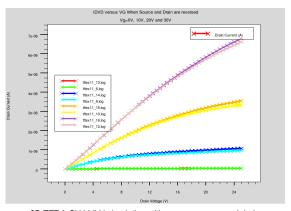
showing the kink suppression effect.

TFT Application Example

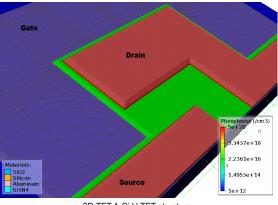
This layout-driven 3D n-type A-Si:H TFT simulation demonstrates specific 3D effect in the IdVd curve when the source and drain contacts are reversed.



3D TFT A-Si:H IdVg simulation.



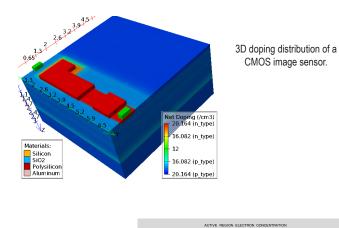
3D TFT A-Si:H IdVd simulation with reverse source and drain.



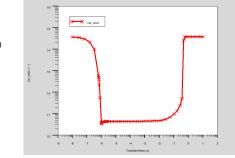
3D TFT A-Si:H TFT structure.

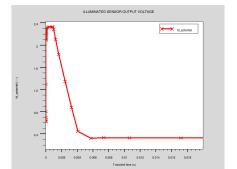
CMOS Image Sensor Application Example

3D process and Device simulation showing transient response of a CMOS Image Sensor under dark and illumination condition.



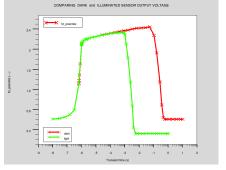
Active region electron concentration under dark conditions.





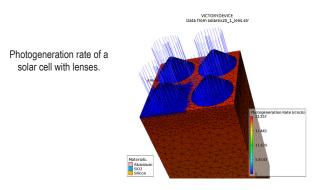
Illuminated sensor output voltage.

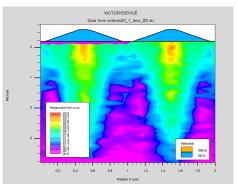
Comparison of dark and illuminated sensor output voltage.



Solar Cell Application Example

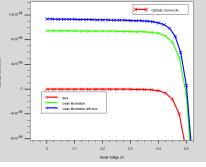
3D Process and Device simulation comparing the IV characteristics of a 3D solar cell with and without lenses. The 3D process simulation starts from a mask and consist of a deposition and angled etch of an oxide layer on top of silicon in order to define oxide lenses. The shape of the lenses can be adjusted as a function of mask size and angle used during the etch. The device simulation uses 3D ray-tracing to take into account the optical reflection, refraction and attenuation and shows that the reflectivity (absoption) is higher (lower) without lenses.





2D cutplane of photogeneration rate.





IV curves with and without lens

0.9 _ Reflectivity Absorption 0.8 _ 0.7 0.6 _____ 0.5 0.4 0.3 _ 0.2 0.1 0.4 0.5 0.6 0.7 0.9 1

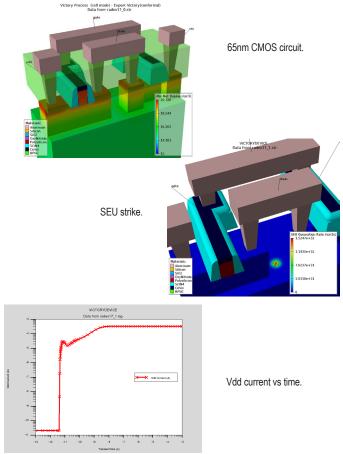
RAT with and Without I

Reflectivity, Absorption and Transmission vs. wavelength.

Radiation Application Example

3D Process and Device simulation of single event 65nm CMOS inverter latchup

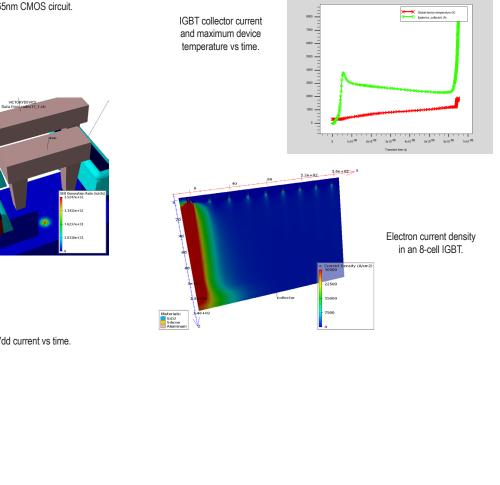
A common issue for any CMOS circuit is the existance of a parasitic thyristor resulting from the NPNP structure that exists between any complementary pair source/drain contacts. This example investigates the latchup effect of a Single Event Upset (SEU) strike on the CMOS circuit.



IGBT Power Application Example

When an IGBT is turned on in the presence of a short-circuit in an output circuit, it can dissipate power in the form of heat to such an extent that current filaments evolve in a localized area within the IGBT device. The heating effects of current filaments are destructive and thus should not be allowed to arise during a short-circuit operation of an IGBT. In this example, a 3D MixedMode short-circuit simulation is performed on an IGBT composed of 8 cells to demonstrate the occurrence of current filaments in a multi-cell IGBT.

VICTORYDEVICE





SILM

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