SmartSpice
Analog Circuit Simulator

SILVACO

Overview

SmartSpice delivers the performance and accuracy required to design complex high precision analog circuits, analog mixed-signal circuits, analyze critical nets, characterize cell libraries, etc. SmartSpice is compatible with popular analog design flows and foundry-supplied device models.

Features

- HSPICE™ and Spectre™ compatible for netlists, models, analysis features, and results
- Provides accurate circuit simulation results for critical analog designs
- Mutli-threading and multi-CPU support for fast circuit simulation
- Multiple solvers and stepping algorithms for robust convergence
- Largest collection of calibrated SPICE models for traditional technologies (Bipolar, CMOS) and emerging technologies (TFT, SOI, HBT, FRAM, FinFET, etc.)
- Provides open model development environment and extensive analog behavioral capability with Verilog-A
- Enables SEE (Single Event Effects) reliability analysis for nanometer scale designs
- Silvaco's strong encryption is available to protect valuable customer and third party intellectual property
- Unique rubberbanding feature that allows designer to modify model, instance and user-defined parameters and interactively see in SmartView how the simulation changes in real time

Accuracy

SmartSpice is the most accurate circuit simulator for critical analog designs incorporating nanometer effects in advanced FInFET nodes.

- Verifies and validates Berkeley physics-based model parameters at run-time for continuity, linearity, and valid parameter range
- Detects inconsistencies in poorly-extracted foundry models and prevents these errors from degrading the final product performance and accuracy
- Offers a full set of options for controlling speed vs accuracy of simulationsof simulations

Speed

- Simulates at 2 to 4 times the raw speed of other SPICE products
- Network distributed SmartSpice and remote .ALTER
- Network distributed Monte Carlo analysis
- Effective parallelization using pool of threads

Convergence

SmartSpice selects the right solver for optimal convergence.

- Surveys initial conditions and iteratively sequences through a series of methods and algorithms to attain optimal convergence
- Multiple solvers provide the best solver for a given circuit topology

Analysis

SmartSpice offers user-defined support for analysis options.

- Stop/Continue algorithm for transient analysis
- Nested parametric analysis
- Scoping of names used in netlist
- Fast cell characterization via direct matrix access on the next parametric step
- Sophisticated optimization at the sub-circuit level
- SEE analysis using .RAD statement leveraging foundry supplied compact models
- Equation editor for .MODEL parameters to support nanometer designs

Ease of Adoption into an Existing Design Flow

SmartSpice fits your design flow and foundry models.

- SmartSpice can co-exist in an existing design flow implemented with HSPICE and Spectre
- Supports foundry-supplied HSPICE and Spectre models
- Supports legacy netlists for HSPICE, PSPICE™, and Berkeley SPICE
- Seamless integration with Cadence analog environment through ADE with SmartSpice run in Spectre compatible mode
- User can run job submission software (LSF, Sun Grid, etc.) seamlessly
- Seamless integration with Silvaco tool suite

Model Development Capabilities

- Core competence in SPICE modeling, data acquisition and model parameter extraction since 1984 with Utmost for the highest accuracy in analog models
- Verilog-A models offer fastest method for implementing Accellera standard electric-thermal models, sensor models, and other mixed physical effects. A Verlilog-A debugger is incorporated to aid custom model development
- Silvaco offers accurate and prompt SPICE Modeling Services to extract DC, AC, S-parameters, capacitance, temperature, noise, and SPICE parameters over full temperature and corner models using statistical analysis

Models Available

BJT/HBT: Gummel-Poon, Quasi-RC, VBIC, MEXTRAM, MODELLA, HiCUM, HBT, HiSIM-IGBT

MOSFET: Level 1,2,3, BSIM1, BSIM3, BSIM4, BSIM6, BSIM-CMG (FinFET), MOSII, MOS20, EKV, PSP, HiSIM, HiSIM2, Level 88, HiSIM_HV, HiSIM_HV2, MOSVAR

TFT: RPI poly-Si, a-Si TFT, UOTFT, MOTFT

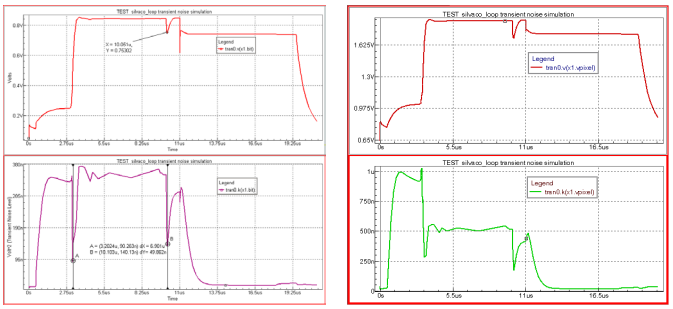
SOI: Berkeley BSIM3SOI, BSIMSOI4, BSIM-IMG, CEA/LETI SOI, LETI-UTSOI

MESFET: Stats, Curtice I & II, TriQuint 1, 2 and 3

JFET: LEVEL 1, LEVEL 2

Diode: Berkeley, Fowler-Nordheim, Philips JUNCAP/ Level 500, HiSIM Diode

FRAM: Ramtron FCAP



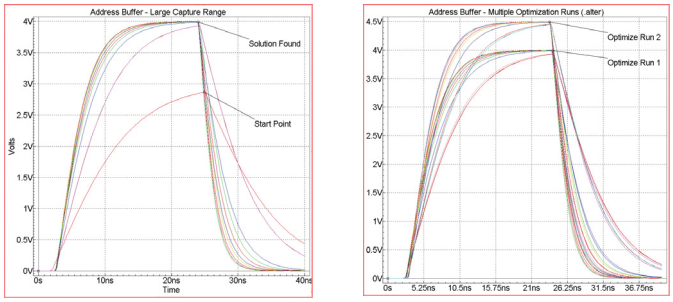
Transient noise simulation: Voltage and noise waveforms at 2 different circuit nodes.

Inputs

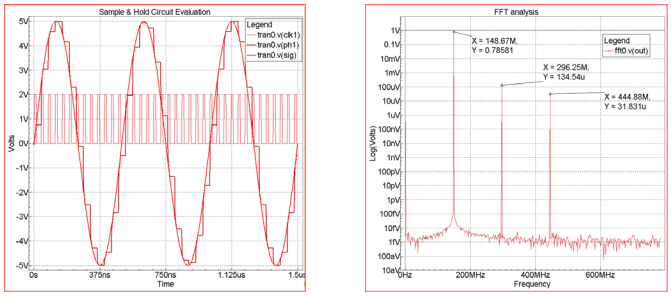
Berkeley SPICE, HSPICE and Spectre netlists, W-element RLGC matrix files, S-parameter model files, Verilog-A.

Outputs

Rawfiles, Spectre PSF, HSPICE tr0 and mt0 , Analysis results, Measurement data, (portable across UNIX/ windows platforms).



Integrated Optimizer iterates device or model parameters to achieve target specifications in the form of DC, AC, transient curves, propagation delay, rise and fall times, power dissipation, etc. Sub-circuit optimization also available.



SmartView: produces annotated plots and graphs of measurements of time, voltage, current, and power for rise time, slope, vector calculator, and eye diagrams from SmartSpice and HSPICE simulation results.