PEX Certify Qualify your Parasitic Extraction Flow

Overview

CAD engineers need to deal with complex parasitic networks, often seen as unfathomable black boxes, with the necessity to ensure the quality and reliability of their extraction flow. The multiplication of extraction flows, versions, and PDKs has an even greater impact on the work to be carried out and the time spent.

PEX Certify was created for this purpose. PEX Certify, composed of PEX Diff and PEX Link, is designed to compare large, extracted netlists to qualify and quantify differences. PEX Certify can very quickly determine if two extracted netlists correspond using statistics and sophisticated analysis of the parasitics without running long-lasting circuit simulations.

PEX Certify is a quality tool. In addition to tasks in the design flow, it can be used to compare different settings of a layout parasitics extraction tool, different versions of the same extraction tool, different formats or even compare different layout extraction tools. The tool is also useful to optimize the settings of LPE flows without completely understanding the extraction algorithms.



Highlights

- Equivalent pin-to-pin resistances
- Equivalent pin-to-pin RC delays
- Inter-nets capacitances
- Statistics

Benefits

- PEX Certify powerful batch mode will seamlessly replace internal verification scripts, often seen as a burden to maintain, and will be able to deal with the complexity and size of advanced designs
- PEX Certify's unique ability to deal with different naming conventions used by different vendors allows CAD engineers to ensure the quality and reliability of their extraction flows
- PEX Certify combined with Viso exploration tool saves weeks of debugging or putting in place the parasitic extraction flows. Parasitic extraction bugs are quickly found and reported
- PEX Certify is not only able to qualify and quantify parasitics related differences, but it also compares devices parameters to ensure the validity of the instance section
- PEX Certify can accurately determines the impact on insertion delay due to manual changes in the routing without running long lasting spice simulation or static timing analysis



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Supported Platforms

• Red Hat Enterprise Linux 7.9, 8.4+, 9.1+: x86_64

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• SLES12 SP5, SLES15 SP3+: x86_64

Input

- DSPF, SPEF, and SPICE parasitic netlists
- CalibreView parasitic netlists
- OA extracted views
- Support of cross-format comparison

Output

- ASCII CSV / TSV results
- Proprietary database for results exploration in the GUI

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Flows

• GUI

APAN

KOREA

TAIWAN

SINGAPORE CHINA

• Command Line Interface

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