Jivaro Pro

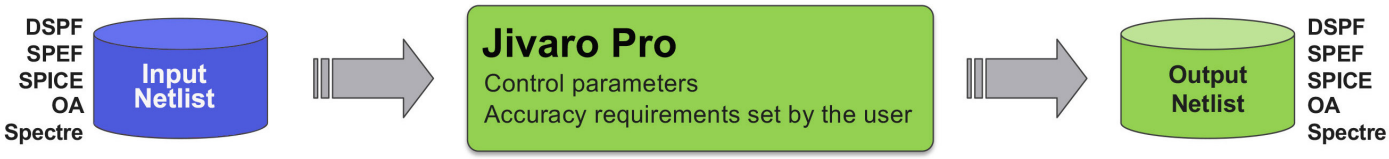
Parasitic Reduction to Accelerate SPICE Simulation

SILVACO

Jivaro Pro is a unique, stand-alone solution dedicated to the reduction of parasitic networks. Jivaro Pro helps back-end verification teams speed up post-layout SPICE simulation of huge extracted parasitic circuits, while maintaining high accuracy.

Jivaro Pro has Proven to accelerate circuit simulation up to 15X faster, while preserving high accuracy.

Jivaro Pro has been adopted at leading IDM and fabless companies worldwide for technology nodes from 65nm down to 5nm. Jivaro Pro applies a patented mathematical approach to perform Model Order Reduction (MOR) to reduce parasitic complexity. In contrast to rules-based methods, Jivaro Pro allows designers to trade off between accuracy and reduction, with the user controlling the benefits.



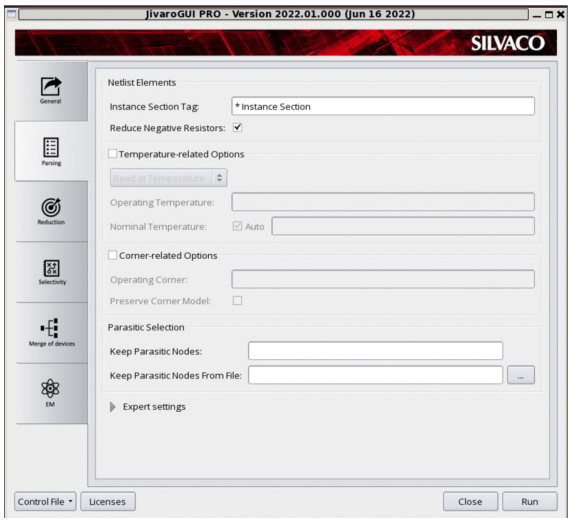
65nm	40nm	28nm	20nm	14nm	10nm	7nm	5nm
✔	✔	✔	✔	✔	✔	✔	✔

Process and technology independent (including FinFET)

Jivaro Pro has no dependencies on the extraction and simulation tools utilized, and can plug directly into any design flow.

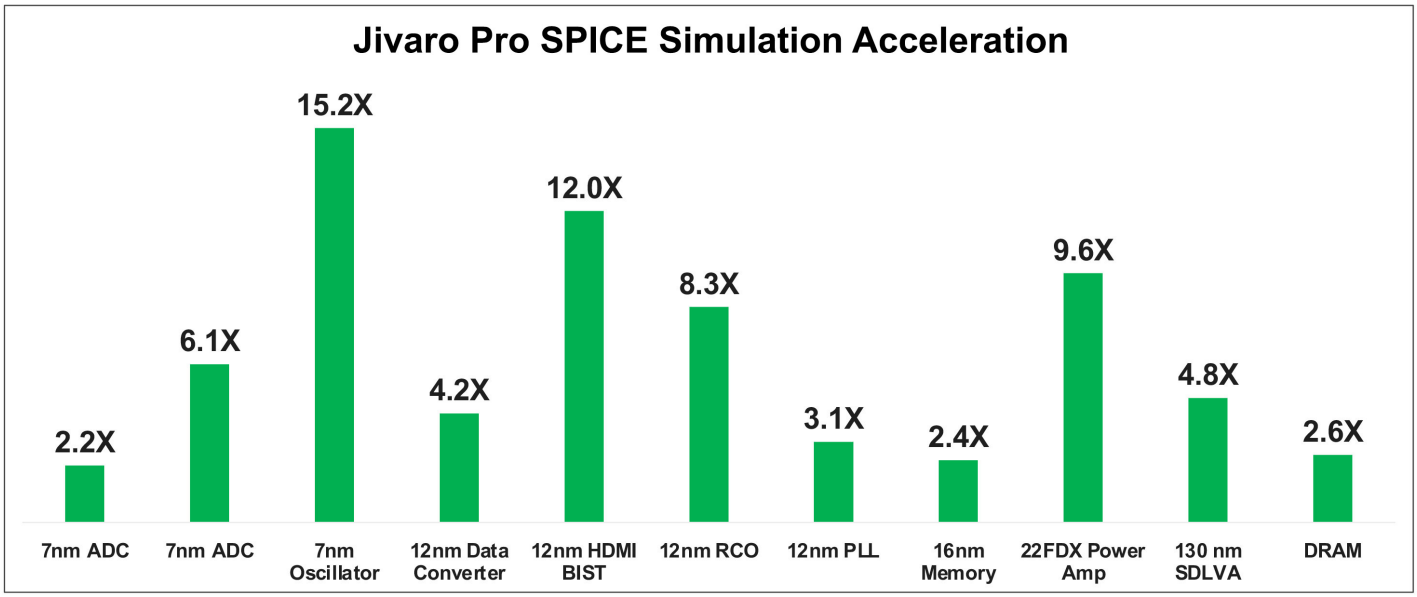
Jivaro Pro contains over 30 parameters that enable broad control over speed and accuracy results. To enable fast implementation and ease of use, Jivaro Pro includes an Automatic Mode capability that adapts and optimizes to your design environment.

Jivaro Pro can be applied with different thresholds on different parts of the design to optimize reduction. It can also offer more than MOR through the reduction of the number of active devices, and can deal with all netlist types, including power nets.

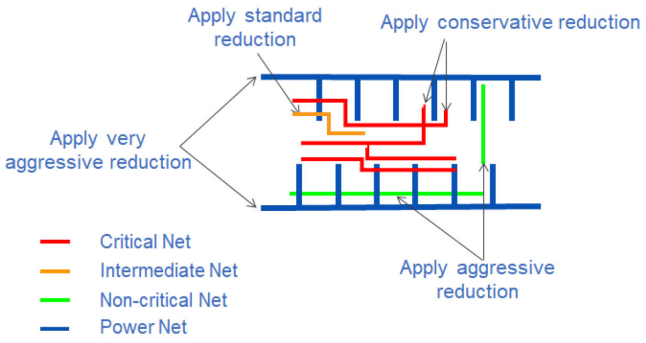


Features

- Accepts R, RC, RCC, RLC, RLCK, controlled sources
- Supports DSPF, SPEF, SPICE3, HSPICE, SPECTRE, CalibreView, OA databases
- Reduces temperature-dependent parasitic networks and multicorner extracted netlists
- Can be applied differently on selected nets, sub-circuits, or any path within the hierarchy
- Merges multi-finger active devices
- Supports negative resistors
- Graphical user interfaces to pilot the reduction options or inline binaries for batch runs
- Compatible with all major EDA tools
- Automatic Reduction Mode
- Automatic Mode triggers advanced features to enable simplified usage:
  - Floating nets
  - Device(s) merging
  - Decoupling of the coupling capacitances
  - Detection and selective reduction of power nets



Jivaro Pro SPICE Simulation Acceleration



Benefits

- Up to 15X post-layout SPICE simulations speedup
- Maintains accuracy to <1%
- Enable the largest or impossible simulations
- Include power nets and metal fills in simulations for more accuracy
- Easy plug and play into existing flow using Auto Mode
- Customize the reduction to your objectives

Supported Platforms

- Red Hat Enterprise Linux (RHEL) 8 – x86, x86_64
- SUSE Linux Enterprise Server (SLES) 11 (SP4) and 12 – x86, x86_64

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