InVar Power - EM/IR - Thermal

SILVACO

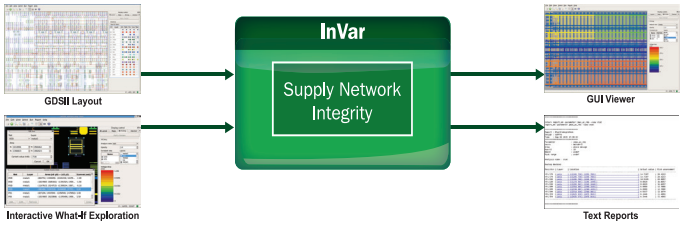
EM/IR, Thermal Reliability and Power Integrity

Silvaco's InVar devised for accurate and effective analysis of designs ranging from block level to chip level. The patented concurrent methodologies provide users the benefits of physical measurement accuracy without delays in runtime, yet also offer the ability of handling extremely large designs. For transistor level designs like analog blocks, high-speed IOs, custom digital blocks, memories, and standard cells, IR-drop, electromigration have traditionally been a bottleneck for physical verification within the EDA industry. Silvaco's hierarchical methodology overcomes that hurdle and more accurately models IR-Drop, electromigration and thermal effects for designs ranging from single block to full-chip across all process nodes, including FinFET technologies.

Power integrity analysis has been typically performed only later in the design cycle where schedule pressures are immense and the range of available design choice is sometimes constricted. InVar Prime provides the ability to perform early analysis on the design, yielding greater design freedom and fewer issues late in the process.

Silvaco's solution utilizes only industry standard design file formats and thus creates a path for users to quickly learn the platform in a user-friendly environment designed to assist quick turn-around-times.

Silvaco's tools were created with the idea of providing true power integrity solution for both early and final sign-off analysis for digital, analog and mixed-signal IC designs.

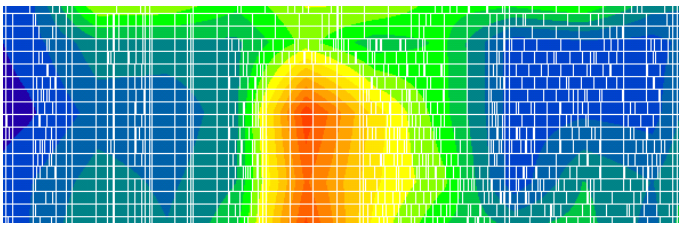


InVar Power

The InVar Power is part of the industry's first real life accurate power analysis platform for transistor-level and gate-level designs. Faster, smaller and cheaper ICs built with expensive process technologies make little room for error, and re-spins are too costly. Silvaco customers are able to tapeout both analog and digital designs correctly and gain most with Silvaco's solutions. Designers can no longer rely on previous generation of analysis/sign-off tools that do not provide complete and comprehensive verification (sign-off) solution. Designers need to understand and analyze all the various effects across the design including mutual dependency between power and thermal 2D/3D profiles, how dynamic thermal profiles affect device behavior in real time, how package, board and even neighboring elements affect realistic electro-thermal design simulation.

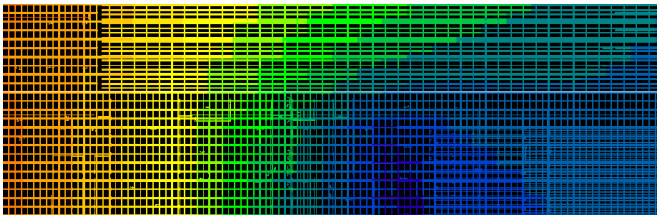
Silvaco's InVar toolset provides a solution that addresses demand for better accuracy and faster verification loops. Taking advantage of parallel processing and advanced algorithms we are able to deliver fast and accurate results matching lab measurements.

The ability to scale to the largest SoC designs while maintaining SPICE level accuracy requires a fundamental change in processing information. Silvaco's solution supports power analysis at device, cell, IP/block. and full chip levels. In case of presence of hierarchical structure of the design InVar Macro Modeling module allows to perform full-chip level analysis in one bottom-up run, accounting for changes in voltage and temperature throughout the hierarchical structure.



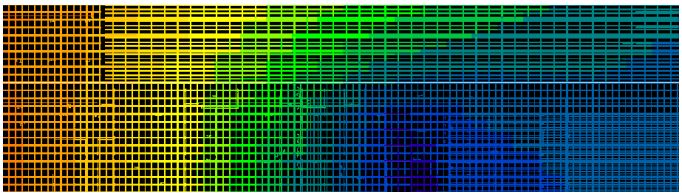
InVar EM/IR

Reliable analysis of EM and IR problems is getting more and more challenging with advanced technology nodes and ever increasing design sizes. Where traditional tools lack scalability, only Silvaco's InVar EM/IR electromigration and IR-drop analysis for analog and digital ICs continues to scale with the complexity and feature size reduction required by modern IC development.



Silvaco provides simple and clear answers to the challenges. With quick and understandable setup it is possible to do analysis for multiple constraints - transient and static, for supply and signal nets in one fast run. Bringing analog and digital blocks together we get analysis to the new level of accuracy, there is no more need for multiple tools with separate and disconnected reports.

InVar EM/IR provides full visibility of supply networks from top-level connectors down to each transistor. Unique approach to hierarchical block modeling reduces runtime and memory and keeps accuracy of true flat run.



Correct support of fast-pacing EM rules represents one of the biggest challenges. Reliability rules are significantly different from fab to fab. This problem does not exist for current users of InVar EM/IR. With flexible programmable implementation and direct support of fab rules user gets support for new rules the same day they get introduced.

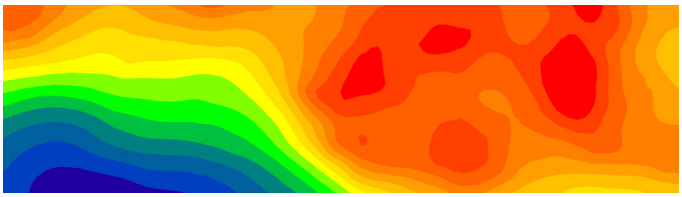
One of the serious problems is a correct support of package models with number of supply pins in the 1000's with exploding die areas . It is not acceptable to reduce package supply to several RLC annotated virtual pins. InVar EM/IR supports RLCK annotation for every supply connector on the die providing ultimate level of accuracy for transient analysis.

InVar Thermal

InVar Thermal provides the industry's largest capacity and most accurate thermal sign-off analysis available today. Silvaco solves the problem of miscorrelation with unique approach to analysis process that is scalable from few transistors to the full chip. Different analysis engines work in concert and take interdependence of power, device parameters, effective supply voltage, and temperature into account. Contrary to other tools, all types of analysis are performed in continuous temperature space across the chip. There are no predefined temperature corners for analysis.

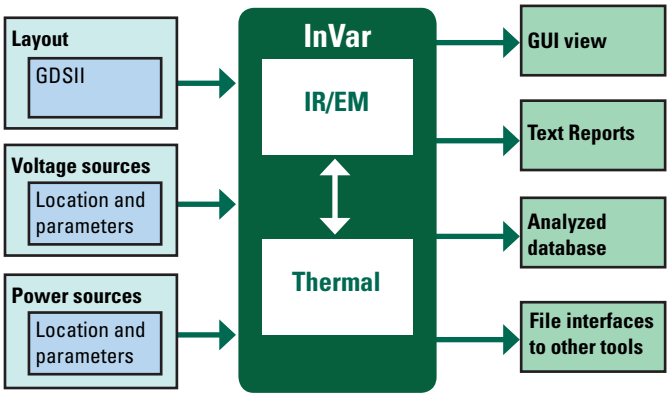
InVar Thermal starts thermal analysis using thermal boundary conditions, environment temperature, and numerous thermal properties that can be individually defined for every material used in design. Analysis continues through fast converging iteration steps and comes up with unique temperature numbers for every device and routing object in the design. That means continuous 2D/3D analysis space for temperature. Patentable technique increases the speed and scalability of analysis engines and gives our customers significant time advantage. User can achieve accurate analysis results with InVar Thermal with less effort due to straightforward, natural flow and use of standard readily available design formats.

InVar Thermal reduces need for other analysis tools from multiple vendors, and our analysis results were verified in customer's labs and outperformed other known thermal tools.



Applications

Early design stage power integrity analysis solution for Layout Engineers. Designers can estimate power, EM/IR and thermal conditions before sign-off stage. It performs checks like resistive parameters of supple networks, point to point resistance and also estimate current densities. It also helps in finding and fixing issues that are not detectable with regular LVS check like missing vias, isolated metal shapes, inconsistent labeling,and detour routing.



InVar for Transistor Level

The transistor-level solution is the only sign-off tool for analog designs that performs concurrent power, thermal and EM/IR checks.

Input data required for Transistor level design:

- Layout- GDSII
- Netlist- SPICE+DSPF
- Technology- ITF or iRCX
- Supplementary data - Layer mapping file for GDSII, Supply net names, Locations and nominals of voltage sources

InVar for Gate Level

Full-chip analysis/sign-off using concurrent analysis of power, thermal, EM/IR on block to full-chip level design.

Input data required for Gate level design:

- Design data- LEF, DEF or Verilog
- Models- Liberty
- Timing- SDC
- Technology- ITF or iRCX
- Activity – FSDB, VPD, SAIF, VCD
- Parasitic file - SPEF

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