## Stivaco I3C IP Selection Guide

|  | MIPI I3C Standard |  |  |  | Silvaco I3C Product Solutions |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | $\begin{gathered} \text { MIPI } \\ 1.0 \end{gathered}$ | $\begin{gathered} \text { MIPI } \\ \text { Basic } \\ 1.0 \end{gathered}$ | $\begin{aligned} & \text { MIPI } \\ & \text { 1.1.1 } \end{aligned}$ | MIPI <br> Basic <br> 1.1.1 | 1.1 <br> Advanced Controller | 1.1 <br> Autonomous Target | 1.1 <br> Advanced Target | Advanced Controller Lite | Advanced Target Lite |
| Product Feature Overview |  |  |  |  |  |  |  |  |  |
| Can operate as I3C Controller | N/A | N/A | N/A | N/A | Y | N | N | Y | N |
| Can operate as I3C Target | N/A | N/A | N/A | N/A | Y | Y | Y | Y | Y |
| APB Slave Interface | N/A | N/A | N/A | N/A | Y | N | Y | Y | Y |
| Simple R/W Interface | N/A | N/A | N/A | N/A | N | Y | N | N | N |
| Supports All Mandatory I3C features | N/A | N/A | N/A | N/A | Y | Y | Y | Y | Y |
| Supports HDR-BT + Multilane | N/A | N/A | N/A | N/A | Y | N | Y | N | N |
| I3C Feature Details |  |  |  |  |  |  |  |  |  |
| 12.5MHz SDR | Y | Y | Y | Y | Y | Y | Y | Y | Y |
| Target can operate as I2C device on I2C bus and as I3C bus using HDR modes | Y | Y | Y | Y | Y | Y | Y | Y | Y |
| Target reset | N | N | Y | Y | Y | Y | Y | Y | Y |
| In-band Interrupt (wMDB) | Y | Y | Y | $Y$ | Y | Y | Y | Y | Y |
| Dynamic Address Assignment | Y | Y | Y | $Y$ | Y | Y | Y | Y | Y |
| Error Detection/Recovery | Y | Y | Y | $Y$ | Y | Y | Y | Y | Y |
| Secondary Controller | Y | Y | Y | $Y$ | Y | N/A | N/A | Y | N/A |
| Hot-join | Y | Y | Y | Y | Y | Y | Y | Y | Y |
| CCCs (required/optional) | Y | Y/N | Y | Y/N | Y/N | Y/N | Y/N | Y/N | Y/N |
| Specified 1.0V operation for 100pf C load | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A |
| SETAASA | N | Y | Y | Y | Y | Y | Y | Y | Y |
| Synchronous Timing Control | Y | N | Y | N | Y | Y | Y | Y | Y |
| Async Timing Control (Mode 0) | Y | N | Y | Y | Y | Y | Y | Y | Y |
| Async Timing Control (Modes 1-3) | N | N | Y | N | N | N | N | N | N |
| HDR-DDR | Y | N | Y | Y | Y | Y | Y | Y | Y |
| HDR-TSL/TSP | Y | N | Y | N | N | N | N | N | N |
| HDR-BT | N | N | Y | Y | Y | N | Y | N | N |
| Multi-lane for HDR-BT | N | N | Y | $Y$ | Y | N | Y | N | N |
| Grouped addressing | N | N | Y | Y | Y | Y | Y | Y | Y |
| Device-to-device tunneling | N | N | Y | N | N | N | N | N | N |
| Multi-lane for SDR | N | N | Y | N | N | N | N | N | N |
| Multi-lane for HDR-DDR | N | N | Y | N | N | N | N | N | N |
| Monitor Early Device Termination | N | N | Y | N | N | N | N | N | N |
| Mapped Addresses | N | N | Y | Y | Y | N | Y | N | Y |

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