# Ultra Low Power Foundation IP GF 55LPx

SILVACO

## Overview

Silvaco's silicon proven Ultra Low Power Foundation IP with industry leading ultra low power Memories and Standard Cells in the GF 55 LPx process enables customers to implement IoT designs for Always ON applications.

Our Ultra Low Power Foundation IP package has a 7T Standard Cell library containing more than 800 cells and Single Port SRAM and ROM Memories. The Standard Cells and Memories are designed with extensive power saving techniques and the SRAM Memory contains extra low leakage modes to ensure the highest power savings at the required performance and area. Customers can use both the Standard Cells and Memories for designing industry leading low power chips in GF 55 LPx.

## Applications


The Internet of things

## Memory

Silvaco's best in class Single Port SRAM in the GF 55 LPx process is designed to achieve minimum area and power while meeting aggressive timing requirements.

The silicon proven memory which uses High Density Pushed Rules foundry bitcell has industry leading low Dynamic Power consumption, and multiple modes for extensive Static Power saving with low leakage.

Other features include Embedded Retention Switch option which provide flexibility and low power operation. It includes Transition Ramp Controller (TRC) that enables control and drastic reduction of the inrush current. Variable write mask and other standard optional features are also available.

## Standard Cells

The Silvaco 7T (seven track) standard cell library provides a highly optimized IP for the GlobalFoundries 55nm LPx node, targeting ultra low power and high-density applications.

The Silvaco 7T Library offers thousands of cells consisting of approximately 650 regular standard cells, more than 150 additional cells for low power and high speed and multiple gate length variants. Most are available in five VTs. They also come in twin/triple well options. This enables designs for applications from ultra-low power to high-speed.

The Silvaco 7T library is extended with a Power Management Kit, taking power reduction to the next level with features such as multi-voltage design and power gating.

## Memory Features and Benefits

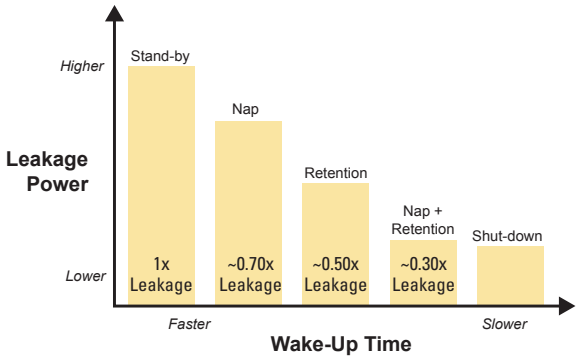
| FEATURE | BENEFIT |
|---|---|
| Multiple Vt periphery | Architecture customized to provide better optimized target power, performance, area envelop |
| Embedded power switches | Saves SoC design time, area, and power while lowering risk |
| Segmented power control | Provides flexibility for segment power shut off and overall power management |
| Read and Write Assist | Low voltage and low power operation |
| Multiple power management modes | Offers multiple power saving customization options |
| Single power supply option | Easy integration |

## Standard Cells Features and Benefits

| FEATURE | BENEFIT |
|---|---|
| Multiple Vt and Well options | Customize designs for optimal low power performance and area implementation |
| Fine grained drive strengths and low leakage cells | Better low power implementation of designs |
| Power Management Kit | Enables power gating and multi voltage low power design methodologies |
| Multi-bit and Multi-height standard cells | Better design implementation with sequential cells and MUX structures |
| ECO kit with fixed pattern for FEOL layers | Enables the flexibility of late layout modifications with minimal number of mask changes |

## Memory Power Management Modes

Multiple power modes for static power savings are available providing the flexibility to select the best trade-off between power saving and wake up time. Retention, retention-nap, and shut-down modes provide a progressive reduction of leakage power compared to stand-by mode.




Leakage data for 4Kx32 instance @ TT, 1.2V, 25°C

Silvaco design architecture enables low power consumption through multiple compiler options.

## Performance of Single Port SRAM GF 55 LPx

| Nbwords x Nbbits | 32 x 32 | 1024 x 32 | 2048 x 32 | 4096 x 32 |
|---|---|---|---|---|
| Area (µm²) | 6034 | 26210 | 49512 | 89103 |
| Acces Time (ns) | 2.2 | 3.17 | 3.31 | 3.09 |
| Cycle Time (ns) | 2.13 | 3.23 | 3.35 | 3.82 |
| | | | | |
| Dynamic Power (uW/MHz) | 2.62 | 4.52 | 5.7 | 7.81 |
| | | | | |
| Leakage Power - Stand-by (uW) | 0.123 | 0.497 | 0.937 | 1.519 |
| Leakage Power - NAP (uW) | 0.122 | 0.359 | 0.657 | 0.958 |
| Leakage Power - Ret (uW) | 0.015 | 0.244 | 0.489 | 0.937 |
| Leakage Power - NAP+Ret (uW) | 0.011 | 0.128 | 0.257 | 0.465 |
| Leakage Power - Shut-down (uW) | 0.006 | 0.129 | 0.264 | 0.537 |

Power data @ (TT, 1.2V, 25°C)

## Standard Cells Low Power Strategies

The Silvaco GF 55LPx Library provides the ability to combine multiple low power strategies to obtain compounded power savings.

- **Power gating** provides coarse grain block shut-down.
- **Level-shifters** enable multiple voltage domains, giving the flexibility of 1.2V and 0.9V operation for optimal performance at low power.
- **Low leakage cells** with long gate channel offer a low static power vs performance trade-off.
- **Fine grain drive** strengths provides more cell options during synthesis, reducing the usage of oversized cells.

| STRATEGY | DYNAMIC POWER SAVINGS | STATIC POWER SAVINGS |
|---|---|---|
| 7 Track | High | High |
| Power Gating | - | High |
| Multiple Voltage Domains | High | High |
| Low Leakage Cells | - | Medium |
| Fine Grain Drive Strengths | Medium | Low |

## Performance of Twin-Well Cells at Multiple VTs

| Process | 55LPX SHVT | | 55LPX HVT | | 55LPX RVT | |
|---|---|---|---|---|---|---|
| Cell | NAND2_X1 | DFFQ_X1 | NAND2_X1 | DFFQ_X1 | NAND2_X1 | DFFQ_X1 |
| Transistors (equiv. gates) | 1 | 6 | 1 | 6 | 1 | 6 |
| Area (µm²) | 1.12 | 5.32 | 1.12 | 5.32 | 1.12 | 5.32 |
| Cell Delay (ps) | 32.84 | 294.82 | 28.47 | 242.52 | 18.66 | 142.27 |
| Dynamic Power (nW/MHz) | 0.71 | 3.20 | 0.74 | 3.29 | 0.68 | 3.04 |
| Leakage Power (pW) | 4.03 | 41.43 | 5.26 | 59.78 | 9.34 | 193.20 |

@ (TT, 1.2V, 25°C)

## Comprehensive Solution

### Trusted Quality

- In volume production with multiple customer tapeouts
- Designed with high-sigma variation analysis to ensure high yield in manufacturing (global and local variation) using Silvaco's VarMan XMA variation analysis tool

### Excellent Support

- Supports major EDA tool flows
- Custom PVT support
- Fast and efficient technical support

Silvaco Memory and Standard Cells in GF 55 LPx are in volume production at multiple customers. Silicon report is available for Standard Cells.

Silvaco offers a 30 day evaluation where customers can get access to Front End + LEF kit for PPA analysis. Contact a Silvaco representative for information.

For more information, please contact us at ip@silvaco.com.

SILVACO
HEADQUARTERS
4701 Patrick Henry Drive, Bldg #23
Santa Clara, CA 95054

NORTH AMERICA sales@silvaco.com
BRAZIL br_sales@silvaco.com
EUROPE eusales@silvaco.com

JAPAN jpsales@silvaco.com
KOREA krsales@silvaco.com
TAIWAN twsales@silvaco.com
SINGAPORE sgsales@silvaco.com
CHINA cn_sales@silvaco.com

WWW.SILVACO.COM

Rev 061721_01