Cello Planar

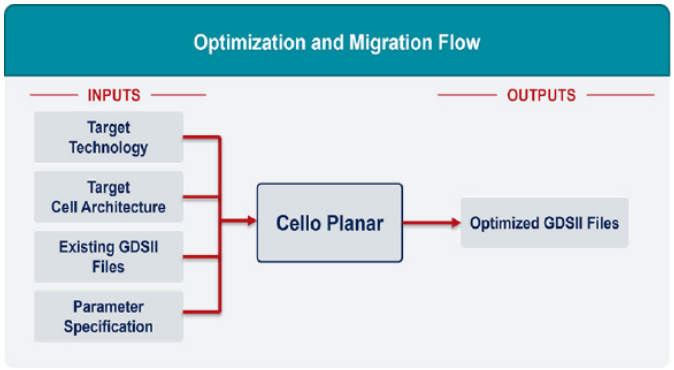
Cell Library Migration and Optimization

Overview

Cello Planar centralizes and automates the design of digital standard cell libraries within a single solution. It provides designers with the ability to control and modify the individual attributes of all cells in a library, allowing for precise adjustments to meet even the strictest design requirements. Cello Planar enables engineers to reuse existing work to fine-tune transistor sizing, row height, design for manufacturability rules (DFM), and other design parameters to manage the trade-offs between power consumption, frequency, and area. Additionally, Cello Planar offers a comprehensive layout customization scripting interface using TCL, integration with third-party verification tools (DRC, LVS, and PEX) with minimal disruption, and flexibility to use within a layout editing flow.

Key Features

- Provides interactive layout DRC cleanup and optimization
- Fast setup of process technologies and foundry design rules, enabling DRC clean layout generation in the first week of use
- Supports advanced process technology constraints, including context sensitive spacing and enclosure rules, preferred shape patterns, and self-aligned double patterning (SADP)
- Flexibility to customize the layout design flow through our TCL scripting API
- Integration with signoff / layout editing environments with minimal disruption to existing flows
- Scalable parallel processing



Cello Planar Flow

Key Benefits

- Improves design efficiency by automating design rule fixing and minimizing manual intervention
- Enables late-stage speed and power optimization
- Migrate layouts between cell architectures and technology nodes that share similar routing structures
- Easily expand your portfolio of libraries exploring different cell architectures, transistor dimensions, and design rules (e.g. DFM)
- Provides a centralized, structured workflow with 2-week ramp-up for new layout engineers
- Consistent library layout, including pin access and block abutment

Advanced Layout Migration

- Supports GDSII-based layout migration
- Provides cell templates to configure cell track height, gate pitch, P/N ratios, size and position of power rails, and cell architecture elements
- Resizes transistors to satisfy new template and drive strength requirements, or to create gate length variants for low leakage applications
- Allows design goal searching through iterative loops

Platform Support

- Red Hat Enterprise Linux® version 7

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