CellForge 3D™

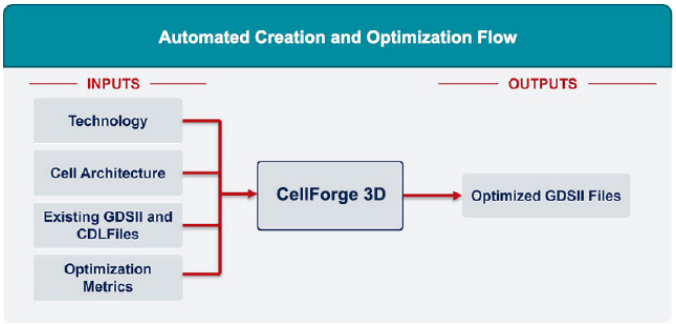
Automated Layout Generation for Advanced Nodes

Overview

CellForge 3D™ tackles the rising challenges of digital standard cell libraries design in advanced and emerging technology nodes. By leveraging the strict constraints of sub-10nm nodes, it offers a solution to automatically generate GDSII layouts from transistor netlists. CellForge 3D provides designers with a framework for exploring and encoding power, performance, and area (PPA) metrics, accelerate library augmentation, and evaluating the impact of design rules and architectural modifications in the layout result. Additionally, CellForge 3D offers a comprehensive layout customization scripting interface using TCL, integration with third-party verification tools (DRC, LVS, and PEX) with minimal disruption, and flexibility to use within a layout editing flow.

Key Features

- Transistor netlist to DRC-clean, GDSII creation
- Support for advanced lithography patterning and design constraints
- Flexible technology modeling for design exploration
  - Single, double, and non-uniform heights
  - Backside power and signal routing
- Integration with signoff and layout editing environments with minimal disruption to existing flows



CellForge 3D Flow

Key Benefits

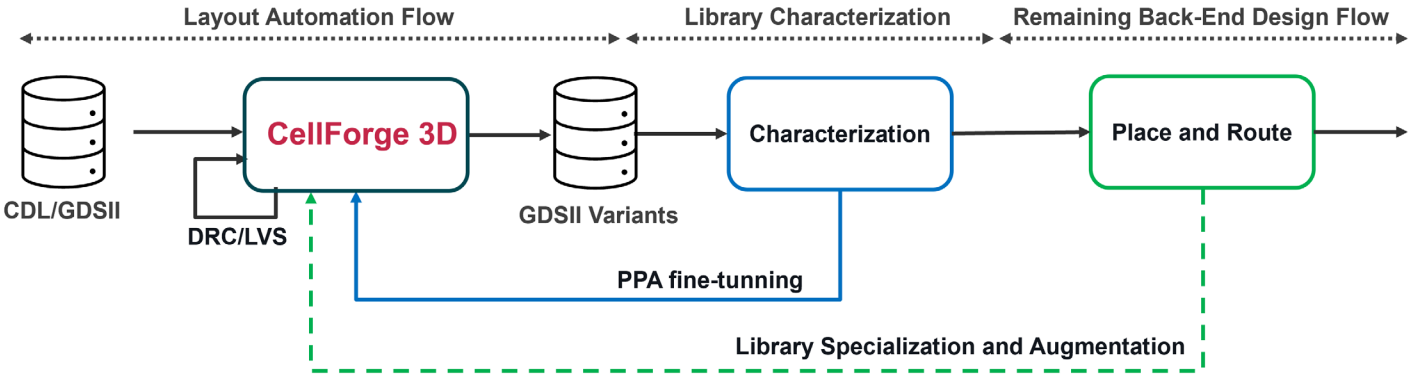
- Significantly improves layout design productivity
- Enables re-routing existing GDSII for DRC fixing or creating additional solutions
- Enables faster design exploration, library augmentation, and DTCO
- Provides a structured, customizable interface for PPA optimization

Multiple Layout Automation Flows

- Library creation from transistor netlist
- Layout updates to DFM/PDK changesn
- Layout PPA optimization
- Cell augmentation and specialization

Platform Support

- Red Hat Enterprise Linux® version 7



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