CellForge 2D™

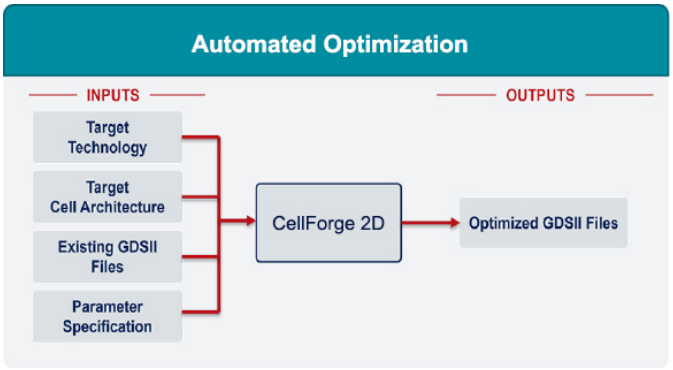
Cell Library Automated Optimization

Overview

CellForge 2D™ centralizes and automates the design of digital standard cell libraries within a single solution. It allows designers to control and modify individual cell attributes, enabling precise adjustments to meet even the strictest design requirements. CellForge 2D helps engineers migrate existing designs, fine-tune transistor sizing, add design for manufacturability (DFM) constraints, and change other parameters to balance design trade-offs. Additionally, CellForge 2D offers a comprehensive layout customization interface using TCL scripting, seamless integration with third-party verification tools (DRC, LVS, and PEX) with minimal disruption, and flexibility within a layout editing flow.

Key Features

- Interactive layout DRC cleanup and optimization
- Migrate layouts between cell architectures that share similar routing structures
- Support for advanced lithography patterning and design constraints
- Flexibility to customize the layout design flow through our TCL scripting API
- Integration with signoff / layout editing environments with minimal disruption to existing flows



CellForge 2D Flow

Key Benefits

- Improves design efficiency by automating design rule fixing and minimizing manual intervention
- Enables late-stage speed and power optimization
- Easily expand your portfolio of libraries exploring different cell architectures, transistor dimensions, and design rules (e.g. DFM)
- Provides a centralized, structured workflow with two-week ramp-up for new layout engineers
- Consistent library layout creation, including pin access and cell abutment

Advanced Layout Optimization

- Supports GDSII-based layout migration
- Enables exploration of cell track height, gate pitch, P/N ratios, and other design features
- Resizes transistors to satisfy new template and drive strength requirements
- Allows design goal searching through iterative loops

Platform Support

- Red Hat Enterprise Linux® version 7

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