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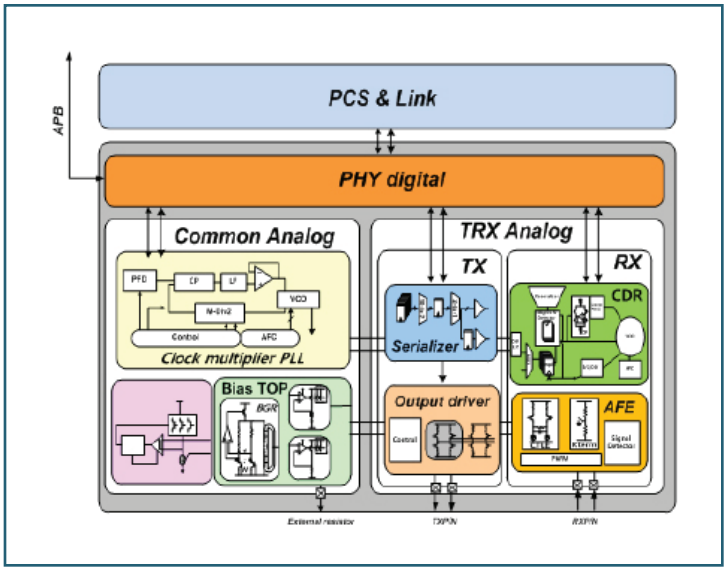
PCIe Gen3 PHY

OVERVIEW

The PCIe PHY IP is a hardmacro PHY for the PCIe protocol. IO pads and ESD structures are included with extensive built-in self test features such as loopback and scan support. It offers a cost-effective and low-power solution. It builds on silicon-proven designs that are in volume production.



KEY FEATURES

- Samsung Foundry 14nm low power CMOS device technology
- 1.8V, 0.8V (or 0.9V) dual power supply
- Compliant to the PCIe Base 3.1 specification
- Supports Gen1, Gen2 and Gen3
- Channel Configuration for Data Lane
  - o Common (CMN) and 1/2/4 Data Lanes
- Supports the following pre-emphasis levels
  - o - 3.5/-6dB for Gen1/2
  - o 3-tap FIR with resolution of 1/36 for Gen3
- 100MHz reference clock
- Supports 100MHz differential clock I/O
- Built-in self test feature capable of producing and checking PRBS random patterns

DELIVERABLES

- Front-end: Timing LIB, Verilog model, Sample test bench
- Back-end: Physical view LEF, GDSII layout, DRC, LVS
- Documentation : Datasheet and User's guide

SAMSUNG Foundry

For more information, please contact us at IP@silvaco.com.

SILVACO

HEADQUARTERS
2811 Mission College Boulevard, 6th Floor
Santa Clara, CA 95054
Phone: 408-567-1000
Fax: 408-496-6080

CALIFORNIA	sales@silvaco.com 408-567-1000
MASSACHUSETTS	masales@silvaco.com 978-323-7901
TEXAS	txsales@silvaco.com 512-418-2929
JAPAN	jpsales@silvaco.com
EUROPE	eusales@silvaco.com
FRANCE	eusales@silvaco.com
KOREA	krsales@silvaco.com
TAIWAN	twsales@silvaco.com
SINGAPORE	sgsales@silvaco.com
CHINA	cnsales@silvaco.com

WWW.SILVACO.COM

Rev 050119_01
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