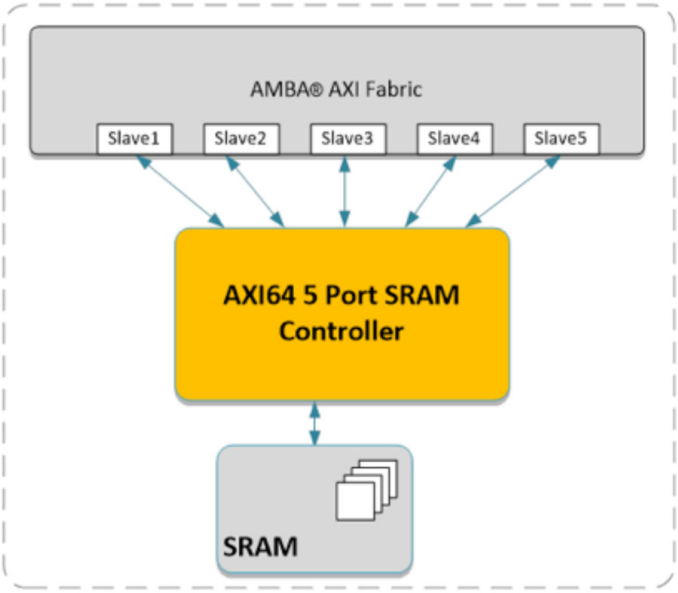
AXI 5-Master Low-Latency SRAM Controller

Overview

The AXI 5-Master SRAM Controller provides 5 AXI 64-bit Masters with low-wait-state access to a single internal 64-bit SRAM resource. It supports low-latency operation by providing access to any memory location within one clock cycle.

The controller decreases latency and improves the throughput for up to 5 Masters accessing a common memory by supporting simultaneous Read/Write access. To achieve this improvement, the memory block is divided into 64-bit segments Access to each memory segment by any of the 5 AXI Masters is arbitrated so that incrementing or wrapping bursts from a given master - the most common types of AXI burst - will not lock out other masters from accessing a given slice for the duration of a burst.



Features

- Allows 5 AXI Masters to access a common 64-bit SRAM
- CPU Master has priority
- Other 4 Masters have equal priority
- SRAM divided into 4 separate slices
- Low Latency with zero or one cycle access
- Fast Arbitration

Deliverables

- Verilog Source
- Complete Test Environment
- Technical Datasheet and Test Document

For more information, please contact us at ip@silvaco.com.

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