

AHB Slave Component to SPI Master Component

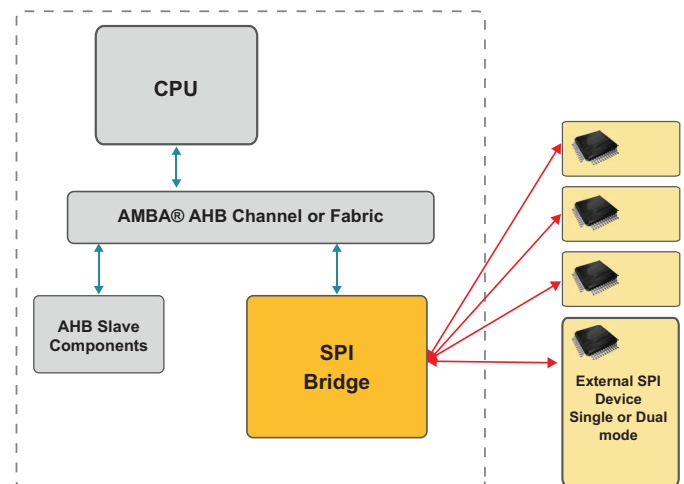
Overview

The AHB-Lite to SPI Bridge is used to translate 32-bit AHB-Lite Writes and Reads to Writes and Reads over a SPI interface. A custom 32-bit protocol is implemented on the SPI bus.

The AHB-Lite to SPI Bridge has two AHB-Lite Slave component interfaces; one for access to the control/status registers (Register Interface), and another for access to the external SPI device (External Interface). The Bridge also has a SPI interface that operates exclusively as a SPI Master component device.

Features

- 32 bit serial transmit & receive
- AHB Configuration Register Interface
- AHB Interface for accessing external SPI device
- Dual-bit or Single-bit mode operation
- Asynchronous SCLK operation
- 32 word Transmit FIFO
- 16 word Receive FIFO
- Interrupt control
- LSB mode
- Support for all SPI modes (CPOL, CPHA)
- Up to 4 Slave components under Master component control



Deliverables

- Verilog Source
- Complete Test Environment
- AHB Bus Functional Model