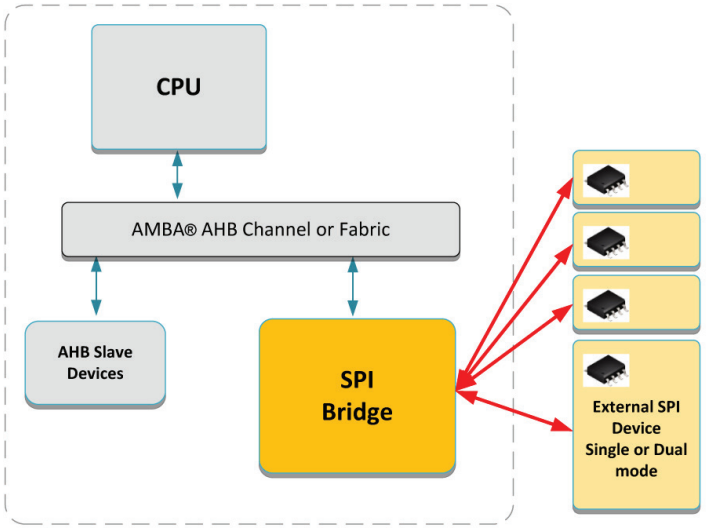
AHB Slave to SPI Master IP Core

DESCRIPTION

The AHB-Lite to SPI Bridge is used to translate 32-bit AHB-Lite Writes and Reads to Writes and Reads over a SPI interface. A custom 32-bit protocol is implemented on the SPI bus.

The AHB-Lite to SPI Bridge has two AHB-Lite Slave interfaces; one for access to the control/status registers (Register Interface), and another for access to the external SPI device (External Interface). The Bridge also has a SPI interface that operates exclusively as a SPI Master device.



AHB SLAVE TO SPI MASTER IP CORE FEATURES

- 32 bit serial transmit & receive
- AHB Configuration Register Interface
- AHB Interface for accessing external SPI device
- Dual-bit or Single-bit mode operation
- Asynchronous SCLK operation
- 32 word Transmit FIFO
- 16 word Receive FIFO
- Interrupt control
- LSB mode
- Support for all SPI modes (CPOL, CPHA)
- Up to 4 slaves under Master control

AHB SLAVE TO SPI MASTER IP CORE DELIVERABLES

- Verilog Source
- Complete Test Environment
- AHB Bus Functional Model
- C-Sample Code

For more information, please contact us at ip@silvaco.com.

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