

Overview

This is a complete implementation of a 16550 UART. The UART contains the following main sections:

- Configuration Registers
- Baud Rate Generator
- Transmitter
- Receiver
- Interrupt Generation Logic
- Modem Control Logic

Configuration registers are written and read by the processor. The baud rate generator produces timing strobes at the baud rate (for the transmitter) and at 16 times the selected baud rate (for the receiver). The UART clock can be asynchronous to the APB clock. The receiver examines the incoming data and uses the first edge of the start bit to determine the bit timing. The transmit and receive paths can be configured to use a single register for data or to use FIFOs. Finite State Machines (FSMs) control the transmit and receive sections. Various error conditions can cause an interrupt to be generated.

Features

- AMBA® APB Compatible
- 16450 and 16550 Compatible Modes
- Modem control
- Programmable baud rates
- FIFO and non-FIFO modes
- Transmit and Receive FIFOs with parameterizable depth
- Interrupt control

Deliverables

- Verilog Source
- Complete Test Environment
- APB Bus Functional Model

