AHB Single Channel DMA Controller

DESCRIPTION

The AHB Single Channel DMA Controller core is a configurable single channel direct memory access controller. The DMA IP Core is a Verilog HDL design that can be used in ASIC, Structured ASIC and FPGA designs. The design is intended to be used with AMBA based systems as a controller to transfer data directly from system memory to memory or system memory to peripheral device or IP Core.

Once set up, the DMA controller is primarily an AHB Master, which initiates data transfers across the AHB bus to/from a peripheral device through the DMA Buffer. The DMA Buffer is a scalable x32-bit FIFO, which is useful for peripheral devices requiring a steady stream of data such as an LCD Controller, Ethernet MAC or other communication device.

The DMA controller contains useful features such incrementing and non-incrementing addressing and link list operation. Linked list support is useful for non-contiguous memory transfer operations.

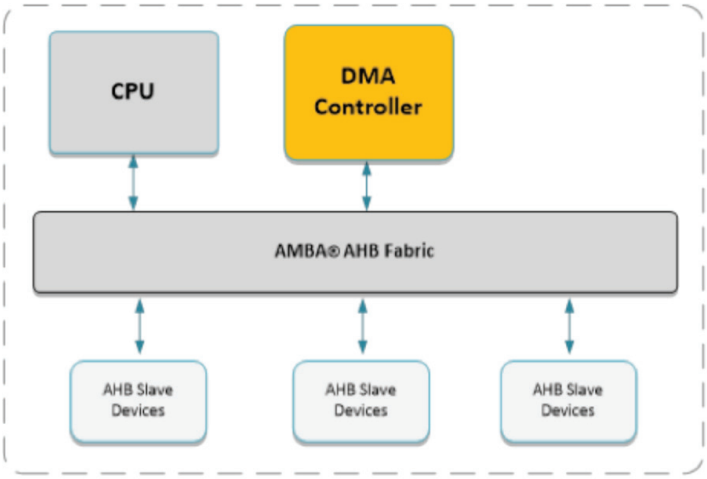
Multiple DMA controllers can be placed in the AHB System to provide multiple channel DMA control.

AHB SINGLE CHANNEL DMA FEATURES

- AHB Master/Slave DMA Controller
- Single Channel – multiple instantiation
- Memory to Memory. Memory to Peripheral, Peripheral to Memory, Peripheral to Peripheral modes
- Source and destination address descriptors
- Single word and burst transfer requests
- Programmable burst size
- Current address status
- Incrementing and non-incrementing addressing
- Linked list support
- Transfer complete interrupt

AHB SINGLE CHANNEL DMA IP CORE DELIVERABLES

- Verilog Source
- Complete Test Environment
- AHB Bus Functional Model



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