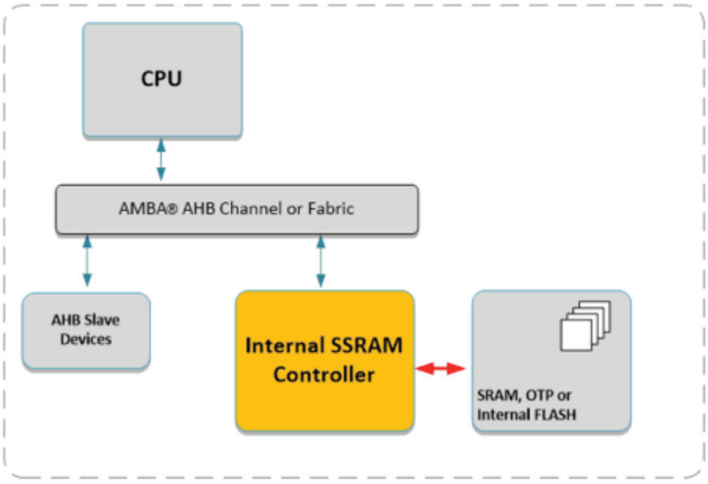
# AHB SRAM Controller

## DESCRIPTION

The AHB SRAM Controller provides a standard AHB interface to translate AHB bus reads and writes into reads and writes with the signaling and timing of a standard 32-bit synchronous SRAM.

The AHB SRAM Controller provides zero-wait-state AHB access to the synchronous SRAM in all cases except for the following back-to-back events: an AHB write directly followed by an AHB read. In this case, a single wait state is asserted. Because of the zero-wait-state operation, this interface is intended to drive an on-chip memory (as opposed to off-chip memory where the return path for the read data might require wait states).

The AHB SRAM Controller contains two interfaces: an AHB Slave interface (for connecting to a Mirrored-Slave interface of an AHB Channel module), and a Memory interface (for connecting to a standard synchronous SRAM).




## AHB SRAM CONTROLLER IP CORE FEATURES

- AMBA® AHB Compatible
- Handles byte, half, and word (8, 16, 32-bit) accesses to internal SSRAM
- Can be used with Internal Flash or OTP Memory
- Zero wait state / low latency operation

## AHB SRAM CONTROLLER IP CORE DELIVERABLES

- Verilog Source
- Complete Test Environment
- AHB Bus Functional Model
- C-Sample Code

For more information, please contact us at ip@silvaco.com.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