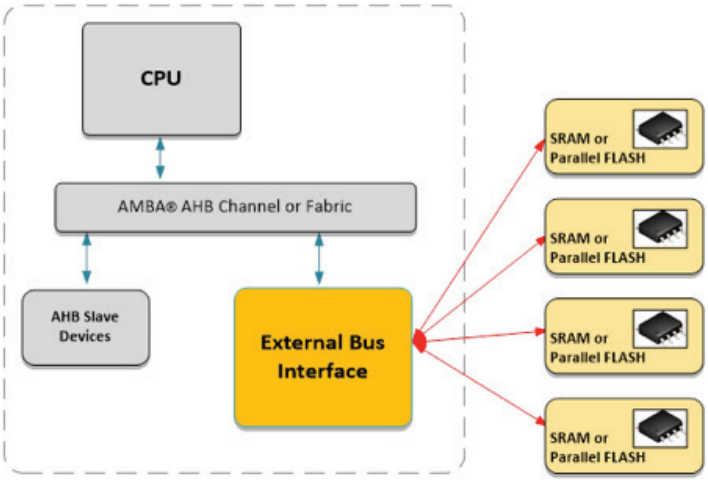
AHB External Bus Interface

DESCRIPTION

The AHB External Bus Interface (EBI) allows a CPU or AHB Master (such as a DMA core) to transmit and receive data to an external device such as an external SRAM or Parallel Flash device.

The number of read wait states, the number of write wait states, and the memory width are all configurable through the APB register interface of the EBI. The EBI allows word, half-word, and byte width addressing to 32-bit, 16-bit, and 8-bit external devices.

The EBI translates AHB writes and reads into writes and reads for the external device. In order to accomplish this task, the EBI is comprised of five major functional blocks: APB Register Interface, Wait State Generation, Address Generation, Control Signal Generation, and Data Steering.



AHB EXTERNAL BUS INTERFACE IP CORE FEATURES

- Interfaces AHB bus to external SRAM or Parallel Flash devices
- AMBA® AHB Compatible
- Supports 8-bit, 16-bit, and 32-bit external modes
- Supports byte (8-bit), halfword (16-bit), and word (32-bit) internal accesses
- Independent programmable wait states per device interface
- Selects up to 4 external devices

AHB EXTERNAL BUS INTERFACE IP CORE DELIVERABLES

- Verilog Source
- Complete Test Environment
- AHB Bus Functional Model
- C-Sample Code

For more information, please contact us at ip@silvaco.com.

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