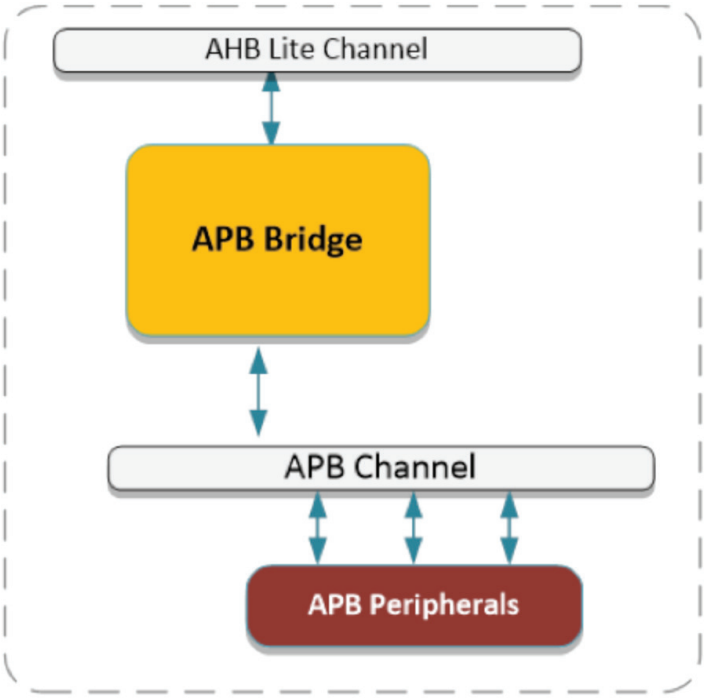
AHB to APB Bus Bridge

DESCRIPTION

The AHB to APB Bridge translates an AHB bus transaction (read or write) to an APB bus transaction. This is accomplished via two small state machines - one on the HCLK domain and another on the PCLK domain.

The AHB to APB Bridge acts as an AHB Slave, and an APB Master in an AHB/APB subsystem. Typically, the AHB to APB Bridge has its AHB interface connected to a Slave port on an AHB Channel module, and its APB interface connected to the Master port on an APB Channel module.



AHB TO APB BUS BRIDGE IP CORE FEATURES

- Translates AMBA® AHB transactions to APB transactions
- Low latency
- Low Gate Count
- Supports APB 2.0 and APB 3.0 Signaling
- Independent HCLK, PCLK pseudo-synchronous clocks

AHB TO APB BUS BRIDGE IP CORE DELIVERABLES

- Verilog Source
- Complete Test Environment
- AHB Bus Functional Model
- C-Sample Code

For more information, please contact us at ip@silvaco.com.

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