AXI to AHB Lite Bus Bridge

Overview

The AXI to AHB Lite Bus Bridge translates an AXI bus transaction (read or write) to an AHB Lite bus transaction. It is expected that the AXI clock and the AHB clock are derived from the same clock source, and that the period of the AHB Lite clock is an integer multiple of the AXI clock in the range [1,16].

Logic on two synchronous clock domains is used to accomplish the translation.

The AXI logic is responsible for responding to transaction requests from the external AXI Master component, and for presenting transaction request information to the AHB Lite logic, and for presenting read data from the AHB Lite subsystem back to the external AXI Master component.

The AHB Lite logic is responsible for generating AHB Lite transactions based on transaction request information from the AXI logic, and for pacing the AHB Lite transaction based on internal FIFO levels and on responses from the external AHB Lite system.

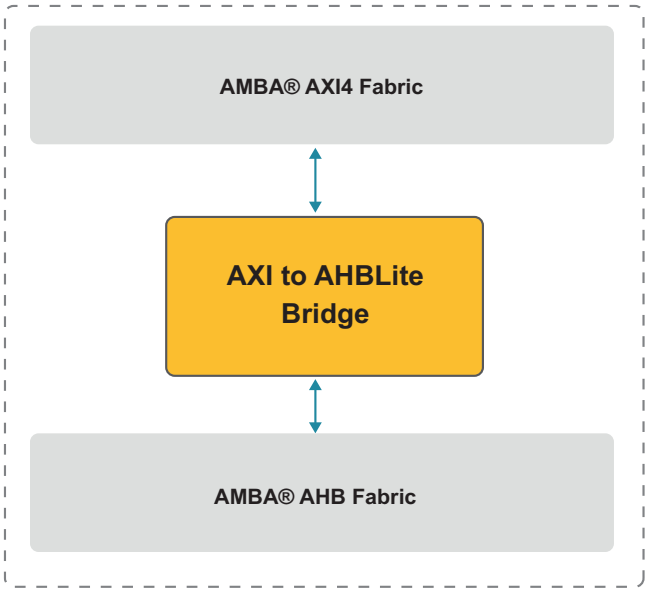
The AXI to AHB Lite Bus Bridge acts as an AXI Slave component, and an AHB Lite Master component in an AXI/AHB subsystem. Typically, the AXI to AHB Lite Bus Bridge has its AXI interface connected to a Slave component port on an AXI Channel/ Interconnect module, and its AHB Lite interface connected to the Master component port on an AHB Lite Channel module.

Features

- Converts AXI Master component transactions to AHB Lite Controller transactions
- Pseudo-synchronous clock domains
- FIFOs for Buffering

Deliverables

- Verilog Source
- Complete Test Environment
- AXI Bus Functional Model



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