AXI Interconnect Fabric

DESCRIPTION

The AXI Interconnect provides the necessary infrastructure to connect as many as 8 shared AXI Slaves to as many as 4 AXI Bus Masters.

AXI defines 5 channels (write address, read address, write data, read data, write response) for its interface signaling between AXI Master and AXI Slave, but does not define a single way that an AXI Master must be connected to an AXI Slave. In general, an interconnect module is necessary when more than one Master and/or more than one Slave is required.

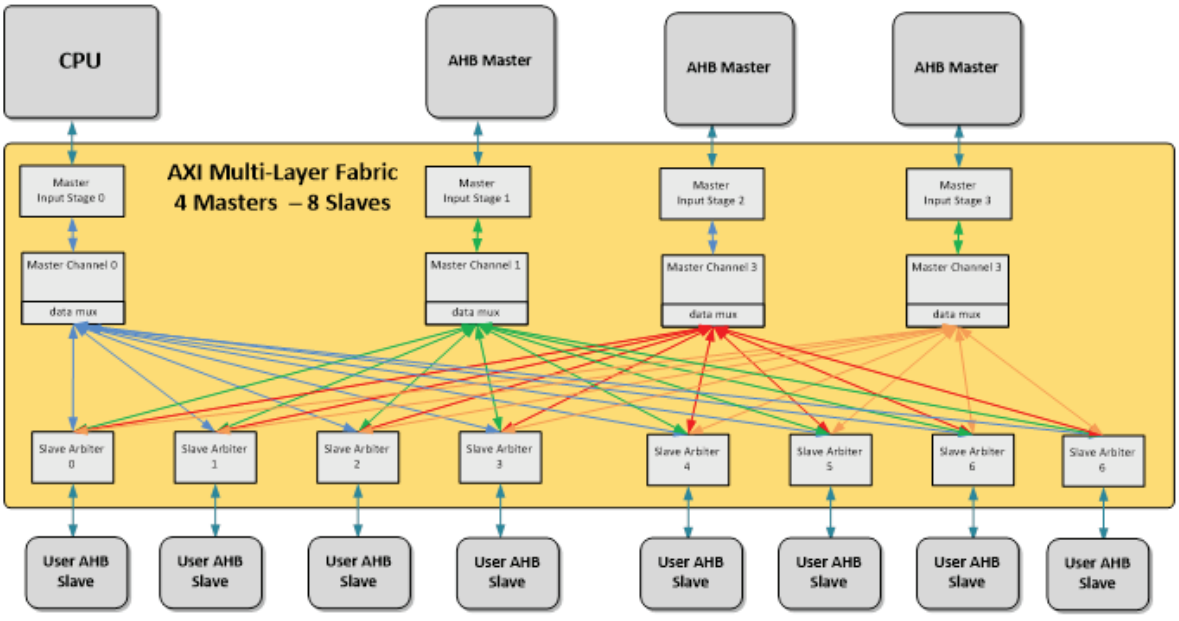
The AXI Interconnect is responsible for routing a transaction from a given Master to the appropriate Slave (decoding and switching), and ensuring that the various Master transactions do not interfere with each other (arbitration.)

AXI MULTI-LAYER FABRIC IP CORE FEATURES

- AMBA® AXI-4 Compatible
- Multiple AXI Channels
- Off the shelf core supports 4 Masters and 8 Slaves
- Arbitration is done at each slave
- Other configurations are available

AXI MULTI-LAYER FABRIC IP CORE DELIVERABLES

- Verilog Source
- Complete Test Environment
- AXI Bus Functional Model



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