

## C166S Processor

The C166S V1 Subsystem is the synthesizable version of the popular C166 16-bit microcontroller plus a rich set of standard peripherals such as general purpose timers and serial ports (synchronous and asynchronous). These tightly integrated peripherals help save power and increase bandwidth by minimizing communication through the external bus interface. The result is a high-performance microcontroller designed for demanding real-time embedded systems applications such as automotive, industrial control, and data communications.

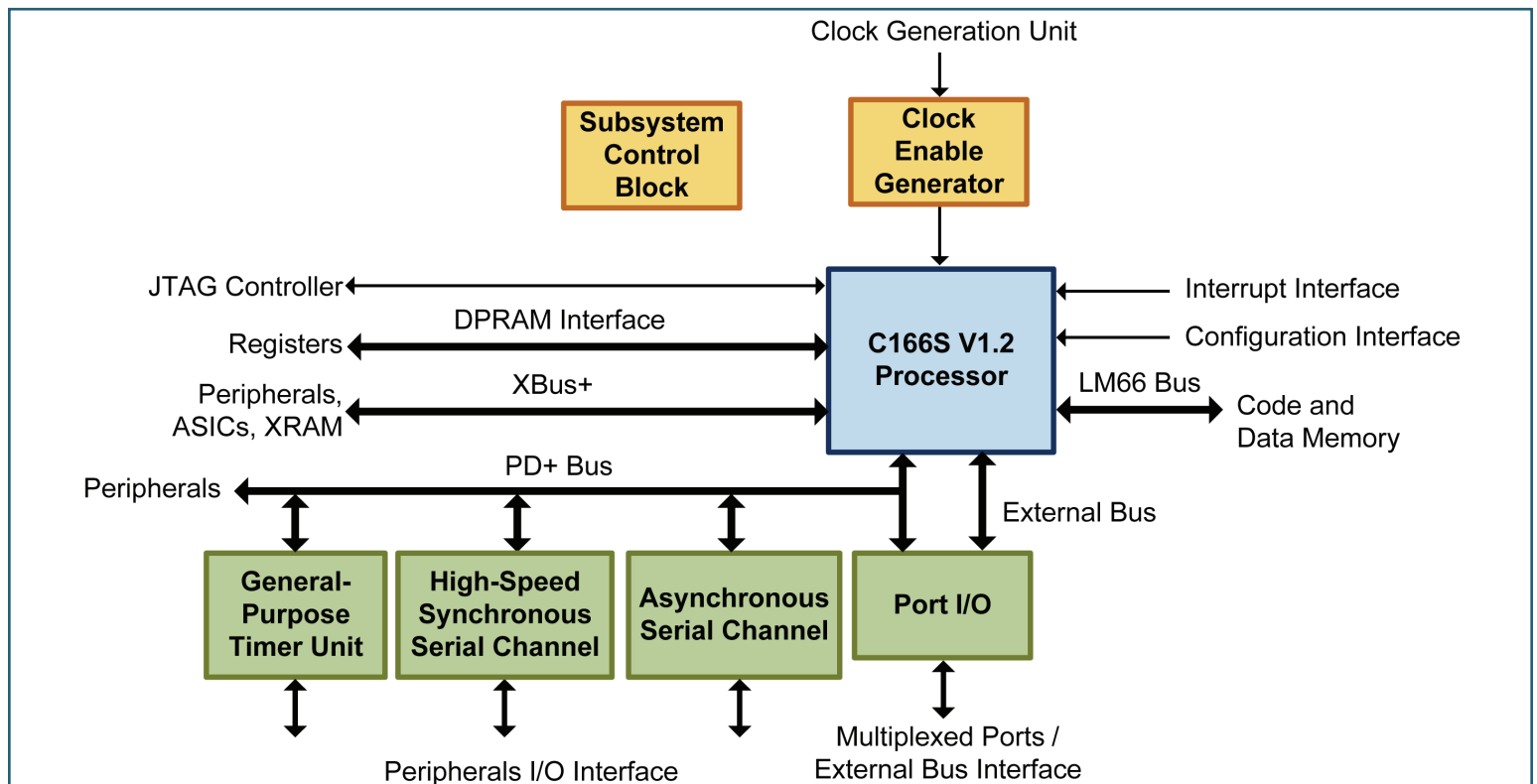
The architecture of the C166S processor combines the benefits of both RISC and CISC (Reduced and Complex Instruction Set Computing). This well-balanced approach delivers the memory saving code density and fast context switching of CISC with the easy RISC instruction decode that enables fast clocking. The C166S processor also features an optional MAC unit to create a unique combination of real-time control and DSP capabilities in one core.

Derived from the successful C166 device family, the C166S V1 Subsystem is fully instruction set compatible with popular Infineon C16x devices and is proven in hundreds of millions of production units.

### C166S V1.2 PROCESSOR FEATURES

The C166S V1.2 processor is the foundation of the C166S V1 Subsystem. Features of the C166S V1.2 processor include:

- 4-state pipelined CPU that is fully compatible with the C166 instruction set
- Optional support for additional MAC instructions
- Infineon On-Chip Debug Support (OCDS) and Cerberus communication channel
- Scalable interrupt controller supporting 12–112 interrupt nodes
- External Bus Controller that supports the Infineon XBus+ protocol and provides support for the off-chip external bus interface



## C166S V1 SUBSYSTEM INTEGRATED PERIPHERALS

The C166S V1 Subsystem builds upon the C166S V1.2 processor, adding several tightly integrated peripherals:

- General-purpose timer unit (GPT12E) that includes 5 multi-functional 16-bit timers for timing, event counting, pulse width measurement, pulse generation, and frequency multiplication
- Asynchronous/synchronous serial channel (ASC) supporting full-duplex asynchronous communication at up to 3.125 MBaud and half-duplex synchronous communication at up to 6.25 MBaud (at 50 MHz)
- High-speed synchronous serial channel (SSC) supporting full-duplex synchronous communication at up to 25 MBaud in master mode and 12.5 MBaud in slave mode (at 50 MHz)
- General-purpose I/O ports. These ports can be used as I/O lines (up to 48) or as the external bus for the C166S V1 Subsystem. The C166S external bus is compatible with Infineon's C166 family of devices.
- Clock enable generator (CEG), which generates the enable signals for the various submodule clocks

## INTERFACES

- Local memory (LM66) bus for single-cycle access to program/data memory
- Dual-port RAM interface for access to register banks, stack, and pointers
- XBus+ for on-chip memories and peripherals
- PDBus+ for on-chip peripherals and external SFRs
- External bus/ports interface for off-chip memories and general-purpose I/O
- Interrupt input signals
- Debug interface
- Clock and reset interface

## DELIVERABLES

- Synthesizable VHDL source code
- Integration testbench and tests
- Documentation
- Scripts for simulation and synthesis with support for EDA tools

For more information, please contact us at [ip@silvaco.com](mailto:ip@silvaco.com).

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Rev 080719\_02  
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