The USB 2.0 High-Speed Host and Device Controller is a highly configurable, synthesizable USB core built from silicon-proven technology from NXP Semiconductors.

The core is an extremely low gate count design that provides an efficient USB implementation in cost-sensitive applications.

It integrates with standard UTMI-compliant PHYs or USB ULPI transceivers on USB side and AMBA AHB interfaces on the system side, supporting all major embedded microprocessor cores.

**Features**

- Compliant to the USB 2.0 specification
- Supports High-Speed (480 Mbps), Full-Speed (12 Mbps), and Low-Speed (Host-only, 1.5 Mbps) operation
- Host and Device functions can switch under software control
- Host is OCHI-compliant
- Two ports available as Host
- DMA engine with connection to AHB interface
- Low gate count (43K gates)
- Various low power features
- Up to 14 non-control logical endpoints
- Bulk, Interrupt, or Isochronous endpoint types
- Maximum packet size 0-1023
- Software-controlled interrupt structure
- Supports single-port RAM for endpoint buffers
- USB buffers can be programmed at the packet or transfer level
- Supported by 3rd-party software (drivers, and so on)
- Independent AMBA AHB-compliant system interface with separate interfaces for Host and Device functions

**Hardware Configuration Parameters**

<table>
<thead>
<tr>
<th>OPTION</th>
<th>RANGE</th>
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<tbody>
<tr>
<td>RAM_ADR_WIDTH</td>
<td>8-15 bits</td>
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<tr>
<td>NUM_ENDPOINTS</td>
<td>0-14</td>
</tr>
<tr>
<td>SINGLE_BUFF</td>
<td>Yes or No</td>
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<tr>
<td>DOUBLE_BUFF</td>
<td>Yes or No</td>
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</tbody>
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**Deliverables**

- VHDL RTL source code
- Test bench with test suites
- Documentation including User’s Guide and Integration Guide
- Technology-independent synthesis constraints