

# M8051(E)W Controller

SILVACO

## Overview

The M8051EW and M8051W microcontroller cores are high-performance versions of the popular 8051 8-bit microcontroller. The M8051EW includes an On-Chip Instrumentation (OCI) debug unit supporting advanced debug operations (start/stop/single-step, breakpoints, and trace) through an IEEE 1149.1 (JTAG) interface. The M8051W does not include the OCI debug unit and, instead, provides limited debug capabilities (start/stop/single-step) through a native debug interface.

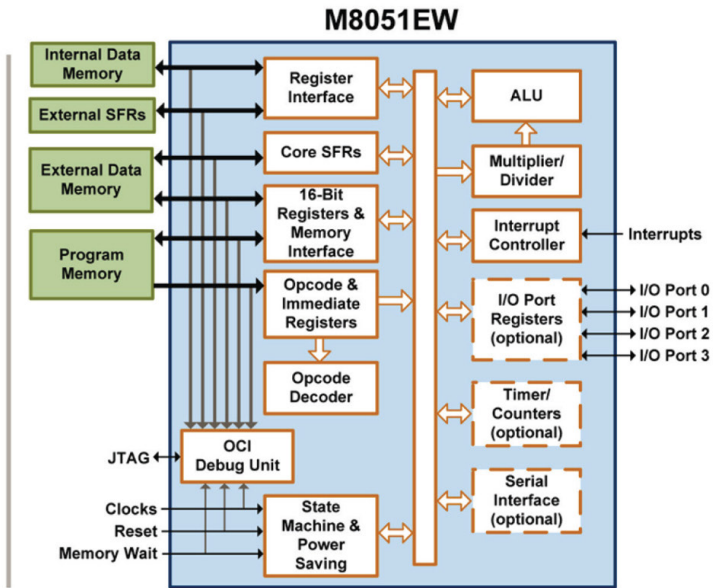
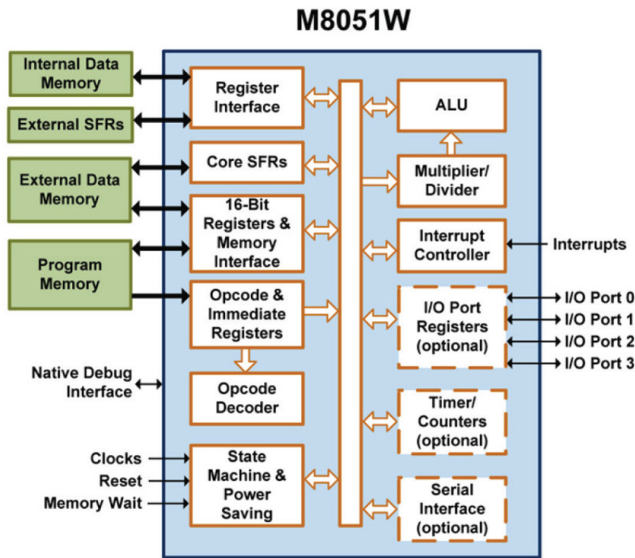
Apart from the debug capabilities, the M8051EW and M8051W are identical. Each requires just 2 clocks per machine cycle instead of the 12 clocks per machine cycle required by industry standard 8051 devices, enabling the M8051(E)W to execute instructions six times faster than standard 8051 devices running at the same clock rate. Or, the M8051(E)W can run at one sixth the clock rate of a standard 8051 device and achieve equivalent performance at a fraction of the power consumption.

The M8051EW and M8051W are microcode-free designs that are software compatible with industry standard 8051 devices, supporting both standard 8051 features and additional features corresponding to Intel 8051, 8031, 80C51BH, 80C31BH, and 87C51 devices and equivalent 8052 devices.

The M8051EW and M8051W each support up to 1 MB of Program Memory and 1 MB of External Data Memory and can be configured to work with either synchronous or asynchronous memories, using either separate Program and External Data Memory interfaces or a single, multiplexed memory interface. Support for slow memories is available through wait states.

## Features

- 2 clocks per machine cycle
- Software compatible with Intel 8051, 8031, 87C51, and 8052 equivalents
- Up to 1 MB of External Data Memory
- Up to 1 MB of Program Memory
- Up to 256 bytes of Internal Data Memory
- Support for synchronous or asynchronous memories
- Wait state support for slow Program and External Data Memories
- Special instruction (MOVC @(DPTR++), A) available for downloading program code to RAM
- Intel-compatible I/O Ports (optional)
- 2 or 3 16-bit timer/counters (optional)
- Full-duplex serial port (optional)
- 25-source, 2 or 4-level interrupt controller with choice of interrupt handling schemes
- 1, 2, 4, or 8 data pointers
- Support for up to 118 user-defined external special function registers (ESFRs), 11 of which may be bit-addressable
- Low-power support through Power-Down and Idle modes
- Fully synthesizable, scan ready design



## Dedicated Memory Interfaces

The M8051EW and M8051W use dedicated interfaces for memory access instead of using I/O ports like standard 8051 devices. Therefore, all 32 of the I/O pins are available for general-purpose I/O.

Internal Data Memory access (up to 256 bytes addressable) is through a dedicated interface to a user-implemented dual-port RAM. Through a configuration option, you can select either a synchronous or asynchronous Internal Data Memory interface.

External Data Memory (RAM) and Program Memory (ROM or RAM) can either use separate memory interfaces or share a single multiplexed memory interface. Both interfaces can be configured to support either synchronous or asynchronous memories. Up to 1 MB of External Data Memory and up to 1 MB of Program Memory are addressable using either a built-in memory extension scheme or standard code banking techniques supported by many 8051 assemblers and C compilers.

## Low Power Support

Separate clocks for the CPU, state machine, and peripherals allow independent shutdown of the associated blocks in different powerdown modes. In Idle mode, the clock to the CPU is stopped while the timer/counters, serial port, and interrupt controller continue to run using a half-speed clock. In Power-Down mode, all clocks are stopped.

## Deliverables

- Verilog or VHDL source code
- Integration testbenches, tests, and simulation scripts
- Documentation
- Scripts for simulation and synthesis with support for common EDA tools