FlexRay Controller

SILVACO

Overview

The FlexRay Controller fully complies with Version 2.1, Revision A of the FlexRay Communication System Protocol Specification. It implements the specification-defined Controller Host Interface (CHI) and Protocol Engine (PE) functionality, with clean partitioning between the CHI and PE functional blocks.

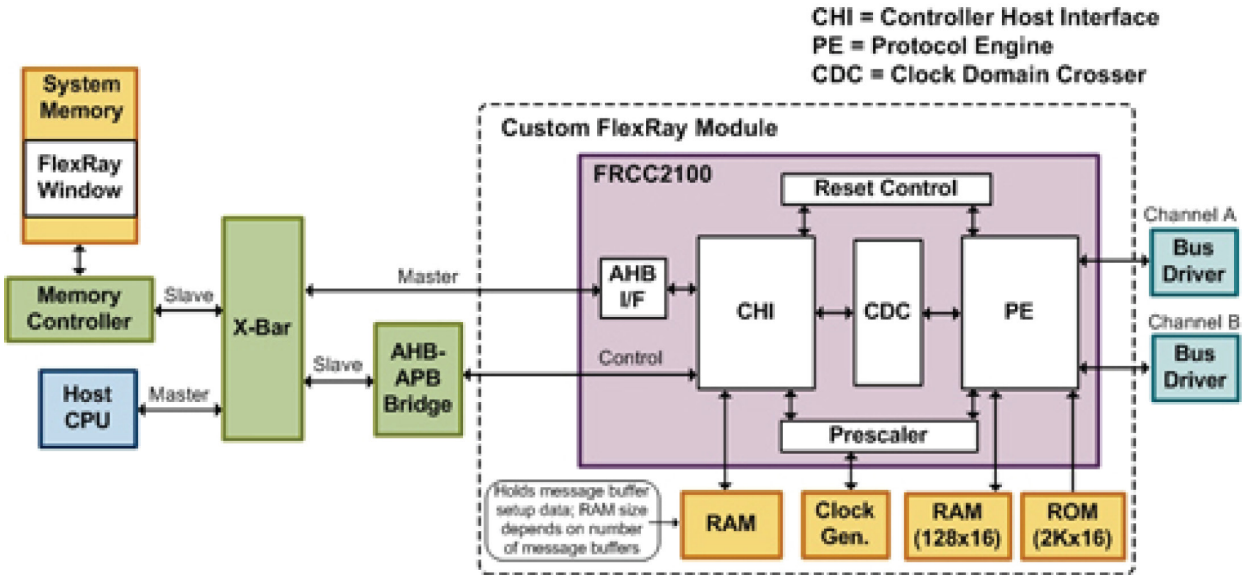
The FlexRay Controller supports 4–252 message buffers and features standard interfaces to system logic and memories, so it can be readily optimized to your system requirements and easily integrated into your FPGA or ASIC device.

The host CPU interface is similar to the AMBA 2 APB. Example glue logic to connect to AMBA 2 APB is included with the product. The interface to FlexRay memory, which stores the message buffer header, payload, and status, is AMBA 2 AHB and can be adapted to other system memory interfaces upon request.

A rich ecosystem, including support from leading FlexRay software providers and a starter kit available for evaluation and prototyping, enables rapid software development.

Key Features

- Modular design
  - o PE cleanly separated from CHI
  - o Memories external to core
- Data transfer is done through message buffers that hold the payload, header, and status information
- Single 10-Mbit/s channel for affordability, dual independent channels for 20-Mbit/s, or redundant 10-Mbit/s channels for reliability
- Support for lower data rates (2.5, 5 and 8 Mbit/s)
- Maskable interrupt signals
- Reports on clock synchronization
- AMBA interface to host CPU and system memory
- Low power consumption through extensive clock gating (optional, may be implemented external to the IP block)
- CHI clock independent of PE clock through Clock Domain Crossing
- Configurable:
  - o Maximum number of message buffers hardware configuration option (4-252)
  - o Message buffer setup programmable at runtime
  - o Two independent receive FIFOs, each with up to 255 entries and flexible filtering
  - o Four configurable slot error counters



Hardware Configuration Parameters

OPTION	RANGE	DEFAULT
Maximum number of message buffers	4-252	32
FlexRay memory (AHB) data bus width	32 or 64 (bits)	32

Gate Count and Performance

NUMBER OF MESSAGE BUFFERS	GATES	MIN. CHI FREQUENCY
4	76,720	32
32	83,431	22
252	140,997	135

Deliverables

- Verilog RTL source code
- Test bench with test suites
- Documentation including User's Guide and Integration Guide
- Technology-independent synthesis constraints

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