# FlexCAN Controller

## Overview

The FlexCAN controller is a highly configurable, synthesizable core implementing the CAN protocol (ISO 11898-1), CAN with Flexible Data rate (CAN FD), and CAN 2.0 B protocol specifications, built from silicon-proven technology.

## Key Features

- Full implementation of CAN FD and CAN 2.0 B
  - Standard/extended data frames
  - Up to 8Mbit/s
  - 0-64 bytes data length

- Compliant with ISO 11898-1

- Flexible mailboxes configurable
  - To store 0-8, 16, 32, or 64 data bytes
  - As receive or transmit

- Individual Rx mask register per mailbox

- Full featured Rx FIFO, stores up to 6 frames

- Transmission abort capability

- Listen-only mode

- Loop-back mode supporting self-test operation

- Programmable transmission priority scheme

- Time stamp based on 16-bit free-running timer with an optional external time tick

- Low power modes with programmable wake-up on bus activity or matching with received frames (pretended networking)

- Transceiver delay compensation for CAN FD Tx at faster data rates

- Detection and correction of memory read (ECC)

- SystemVerilog integration testbench including a number of usage scenarios
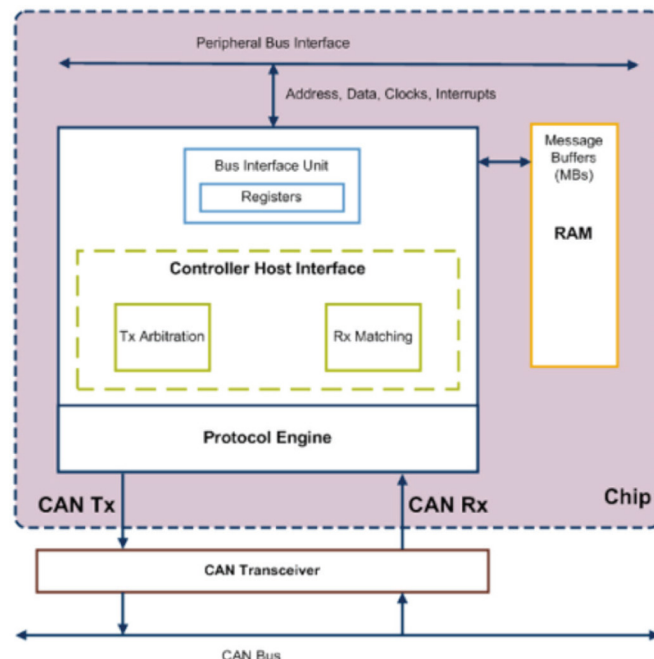


## Hardware Configuration Parameters

| OPTION | RANGE |
|---|---|
| IRMQ_EN | Yes or No |
| LOCK_IRMQ | Yes or No |
| ECC_EN | Yes or No |
| DMA_EN | Yes or No |
| PNET_EN | Yes or No |
| FD_EN | Yes or No |
| NUMBER_OF_MB | 16, 32, 64, 96, 128 |

## Deliverables

- Verilog RTL source code

- Test bench with test suites

- Documentation including User's Guide and Integration Guide

- Technology-independent synthesis constraints

For more information, please contact us at ip@silvaco.com.