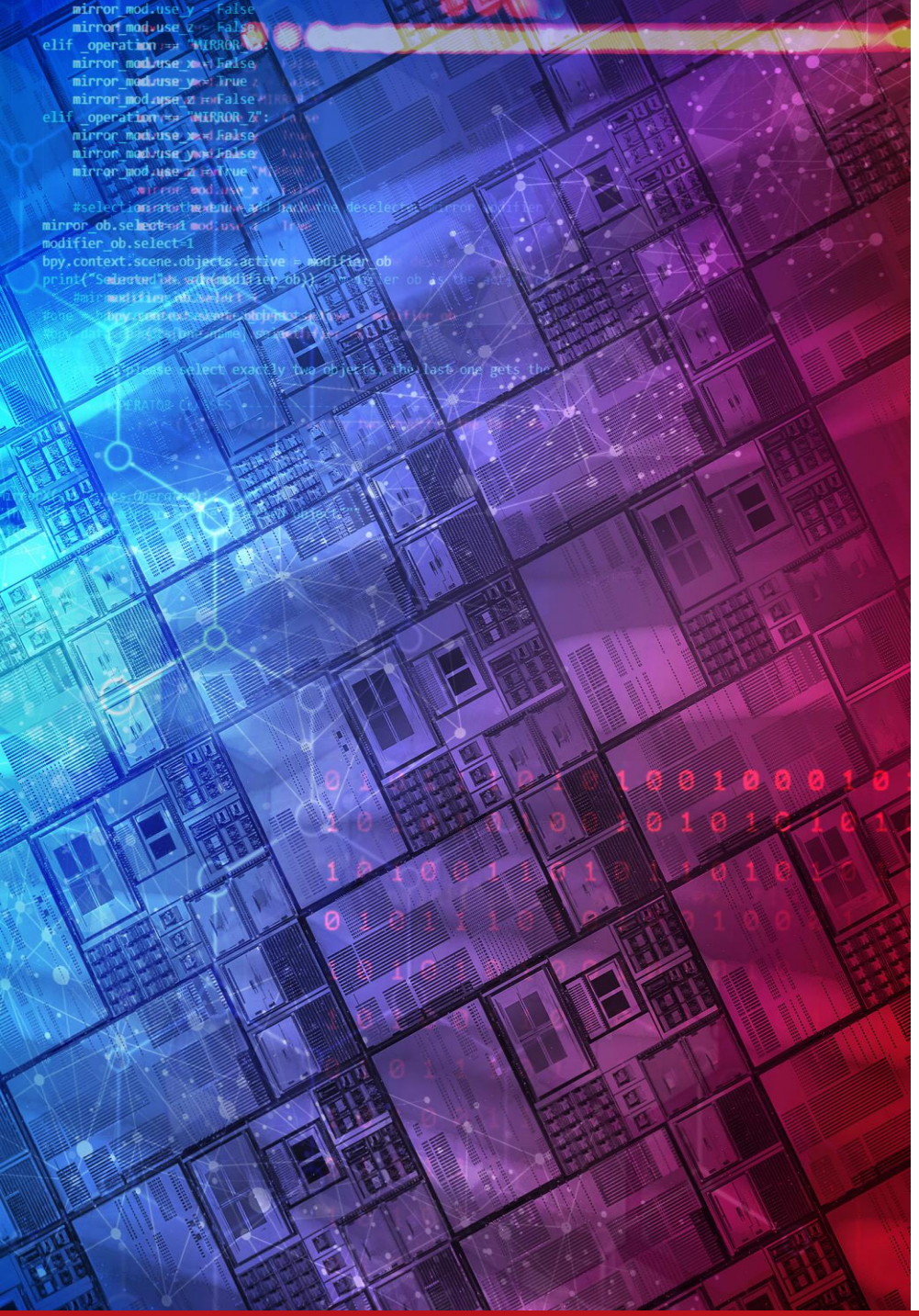


SILVACO

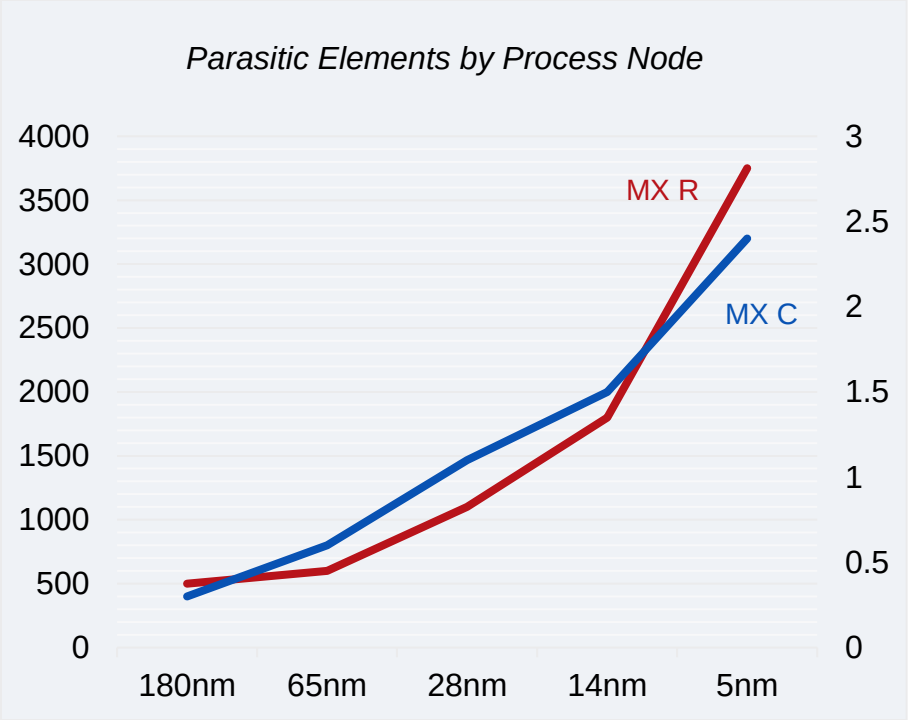
Viso

Parasitics Analysis and Debug

Introduction

Parasitic elements are growing exponentially

- As process geometries grow smaller the number of parasitic elements grow at a dramatic rate
- Interconnects and layout parasitic networks are more and more complex, and often considered as an immeasurable black-box
- Silvaco provides dedicated solutions to highlight and explore these networks and interconnects to debug and optimize your layout



Number of parasitic resistors increased by 3.5X in between 28nm and 5nm.

Introduction

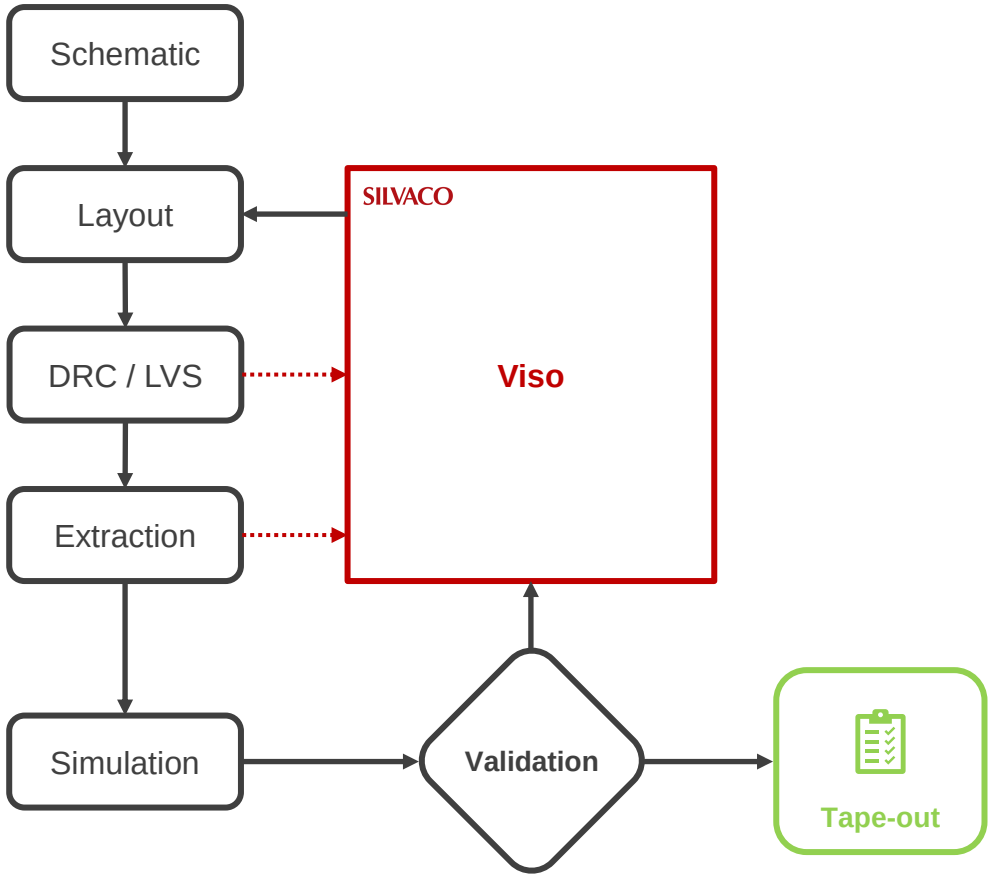
Parasitics are increasing simulation runtimes

- These vast number of parasitic networks can dramatically increase simulation runtimes
- Interpretation of the simulation results and its complexity is often underestimated
- Parasitics can also lead to an overall rethinking of the design flow, optimization and debug which takes way longer than a simulation
- **Viso** eases parasitic extraction flow setup, saves simulation time and enables powerful physical design debug

Viso

Value proposition

- Viso enables users to highlight the design of critical and specific nets
- Provides designers with a fast and easy way to quickly detect potential layout issues early in the design
  - Highlights impacted critical nets
  - Helps explain where the problems are, and evaluate various solutions



Viso

Value proposition

- Including an extensive set of features enables many different approaches to assess the quality of a design
- Within a few seconds, Viso’s sanity checks can prevent wasting hours waiting for doomed simulations
- Viso enables designer to quickly analyze and optimize very large power networks, either for debug or exploration
- Designers can visualize resistance, delay maps, and voltage drops without running long and expensive power simulations

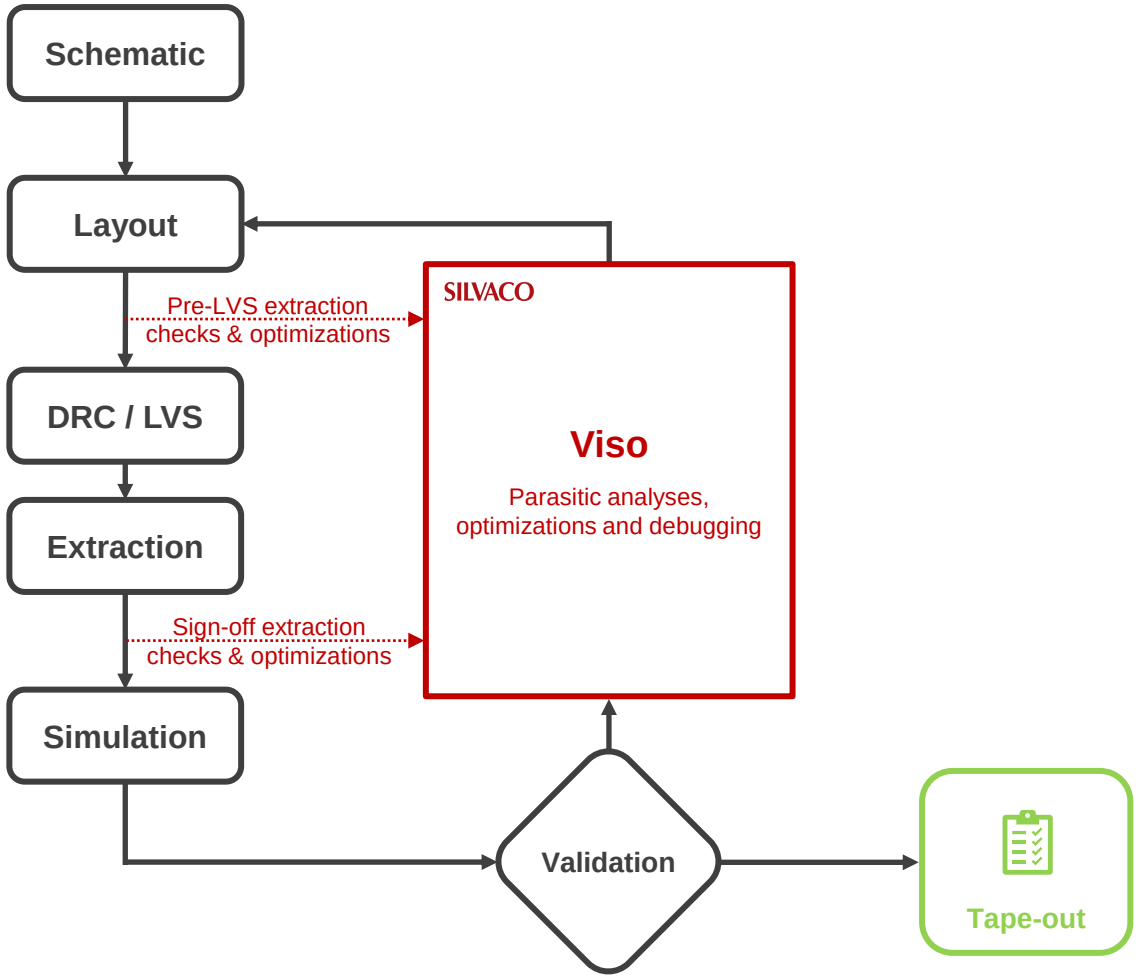
Designers Challenges and Solutions

Debug and optimize your layout

- The primary challenge for layout engineers is to ensure that their layout is reliable and meets the required performance targets
- Detect and highlight sources of design problems is a priority: crosstalk effects, signal weaknesses, unbalanced net symmetries, delay degradations, IR drop issues, etc.
- Designers currently rely on different solutions to validate the integrity of the layout
  - Their own experience to anticipate issues and avoid known controversial patterns
  - Multiple iterations of post-layout simulation to validate each modification
- However, as parasitic effects become increasingly complex to address, the design times lengthen and design costs on advanced nodes grows
- Dedicated tools as **Viso** become essential for design and layout engineers

Viso

A complete and dedicated solution for design and layout engineers



Viso General Usage

Input and outputs

- Computes numerous analyses through 2D / 3D visualization, or directly by command line:
  - Equivalent pin-to-pin resistance per net or across devices (path-tracing), RC delays, crosstalk
  - Access resistance map, voltage map, complex impedance computations
  - Highlight of main contributors, sensitivity, etc.
  - Net comparisons with support for differential signaling and parallel signaling
  - "What-if" exploratory functionality
  - Numerous sanity checks (shortcuts detection, disconnected instances, and more)
  - Multifinger pins merging with tunable initial conditions (voltage or current equivalent)
  - Superimposition of GDSII or OA data over parasitic data, interactions with major design environment

Viso General Usage

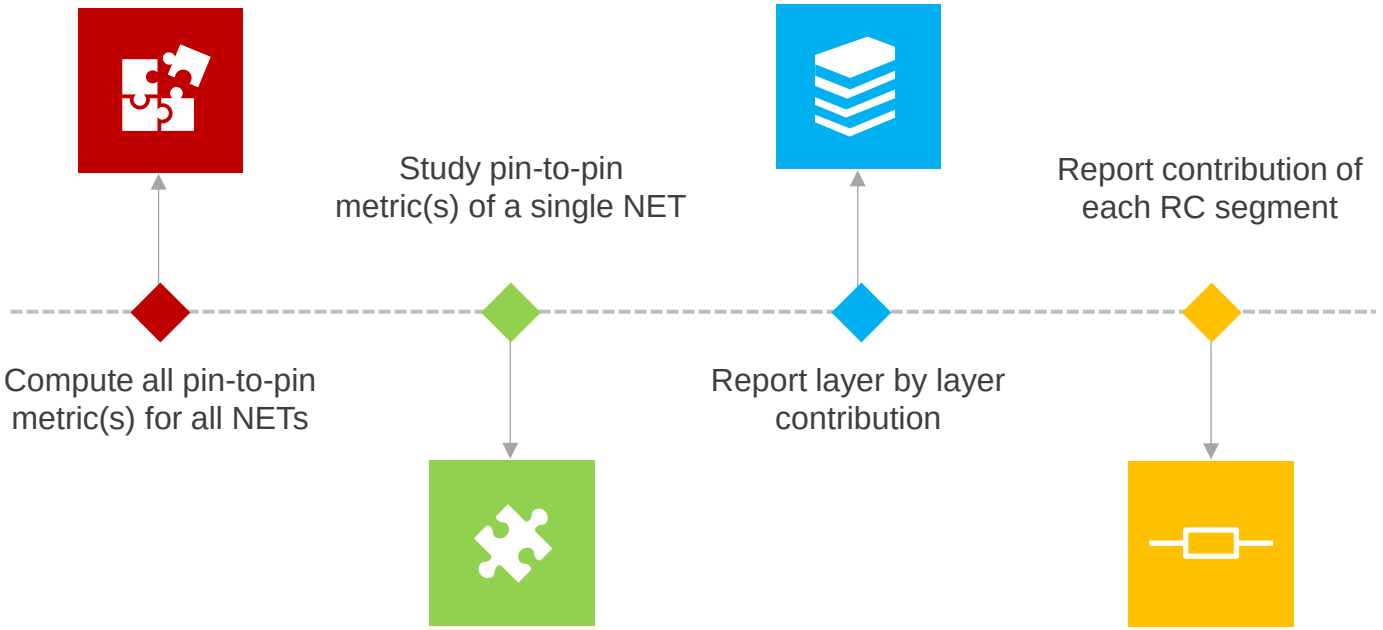
Input and outputs

- All major formats supported: DSPF, SPEF, SPICE, and CalibreView parasitic netlists, OpenAccess extracted views
- Results are detailed in the GUI through different tables, graphs, and colormaps
- Batch results can be outputted in ASCII files (csv, tsv, and more)

A Top-Down Approach

Deep exploration of interconnects

- Viso enables different levels of abstraction
  - From global results for a given metric to a very detailed level.



"What-if?" Investigation

Quick modifications of the layout

- Possibility to perform on-the-fly modifications of the parasitics network before re-running different time-consuming analyses
- Exploration and analyses of the different scenarios created allows to anticipate the results without having to directly modify the layout
- One can remove, add, or change the value of a resistor or via. The resistivity of a complete layer can also be updated

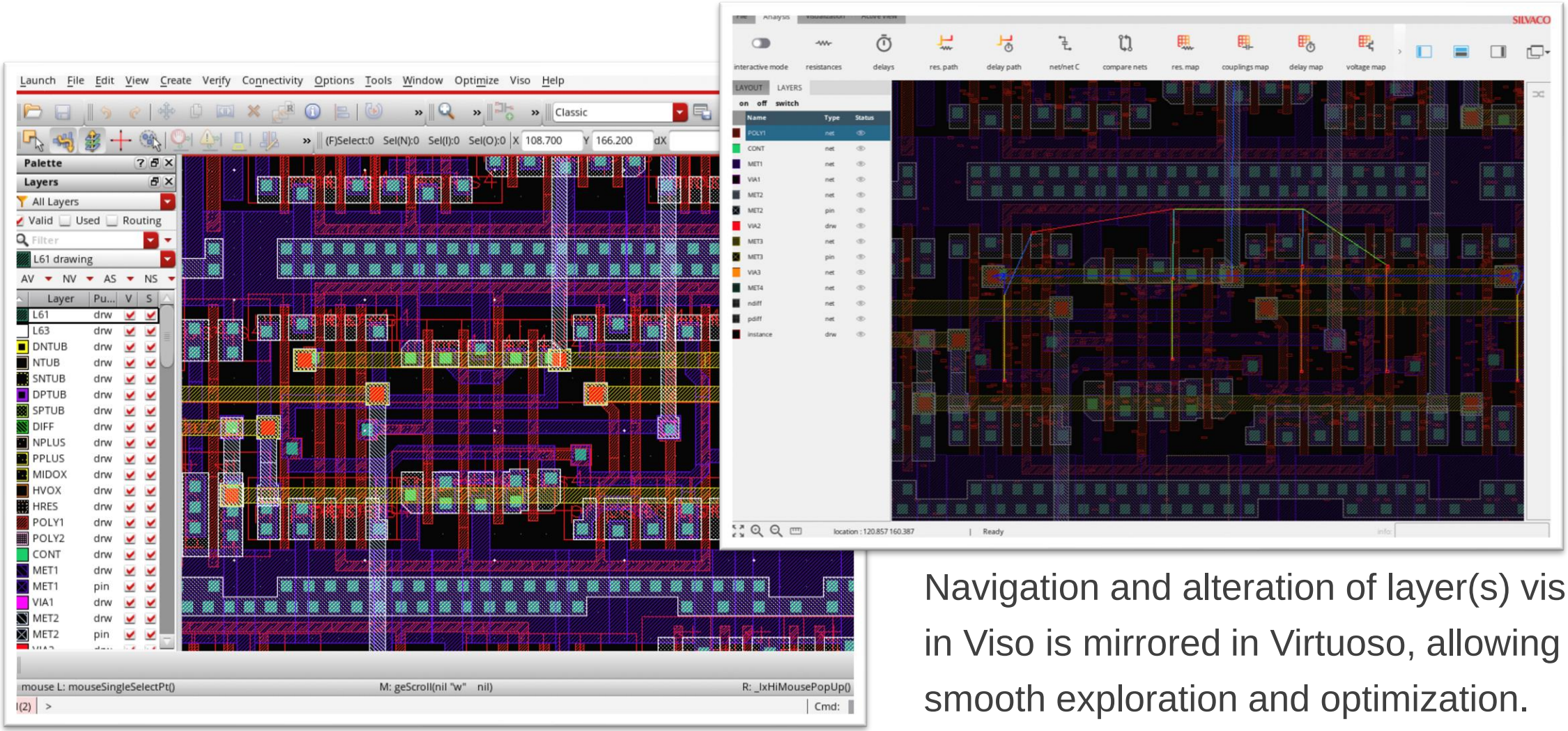
Interaction With Design Environment

Create a link with your layout editor

- Silvaco offers the possibility to create a close interaction between a Cadence environment and Viso graphical user interface
- Viso reads the OA format used to store data in Virtuoso to create the corresponding parasitics view
- Once in place, a direct link exists between the extracted view (or the layout view) in Virtuoso and the corresponding database in Viso

Interaction With Design Environment

Screenshots



Navigation and alteration of layer(s) visibility in Viso is mirrored in Virtuoso, allowing a smooth exploration and optimization.

Viso

Benefits of our solution

- Easy to use and engaging user interface, embedding visual exploration of parasitics and results in 2D and 3D, to accelerate the detection of potential issues
- Allows rapid analysis of multi-GB post-layout netlists
- Interaction with Cadence Virtuoso
- Can be used early in the design flow even on non LVS clean designs
- Powerful batch mode that can be used to implement verification scripts that fit customer flows
- Evaluation of the impact of changes through several scenarios using an embedded "what-if?" feature
- Easy to setup and integrate in flows with no complicated preparations


Thank you
SILVACO