SILVACO

# Jivaro

## Accelerate SPICE simulations by up to 15X

# *Jivaro* Parasitic Netlist Reducer

## Are your SPICE simulations slow???

## *!!! You need Jivaro !!!*

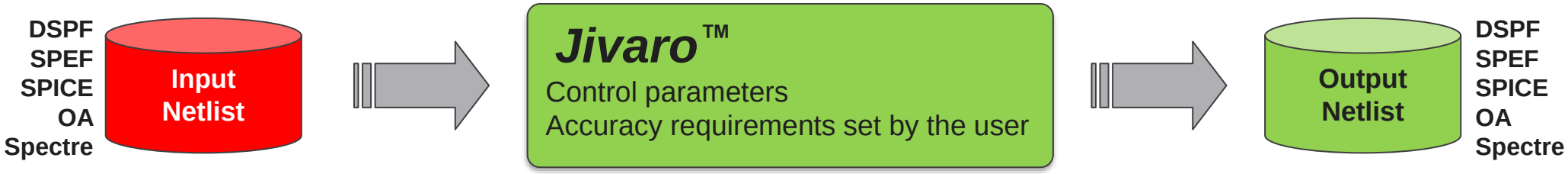
Original simulation runtime

**Up to 15x runtime improvement**

*Jivaro* simulation runtime

# Netlist-in → Netlist-out stand-alone solution

## Process and Technology Node Independent (including FinFET)




- Drastically reduces extracted parasitic netlists (90% +)
  - Reduces R, C, CC, L, K and active devices
- Maintains accuracy to < 1% of original netlist

| 65nm | 40nm | 28nm | 20nm | 14nm | 10nm | 7nm | 5nm |
|---|---|---|---|---|---|---|---|
| ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |

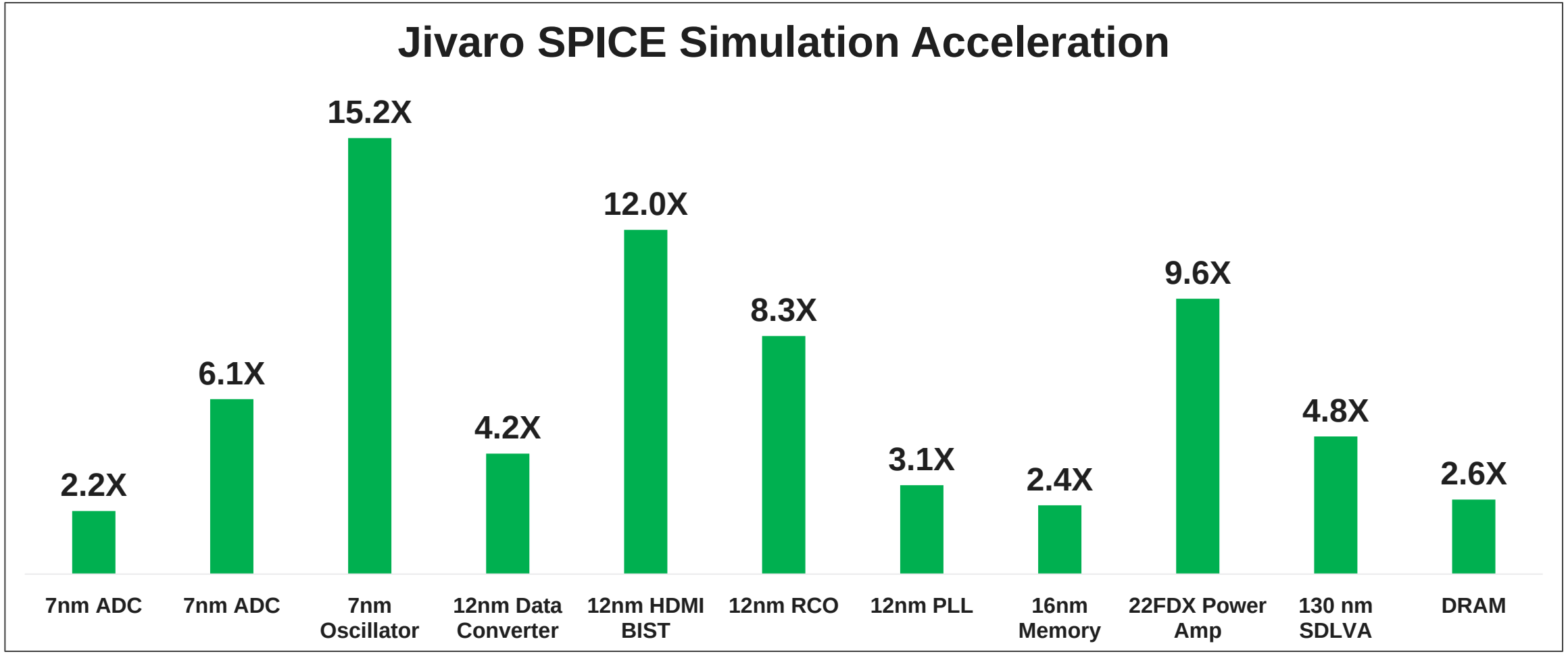
- User can configure accuracy on all NETs, subcircuits and paths independently
- Include power nets/metal fills in simulations for more accuracy
- SPICE simulator independent
- Supports all major input formats

# Jivaro Works for All Design Types

## Design flexibility

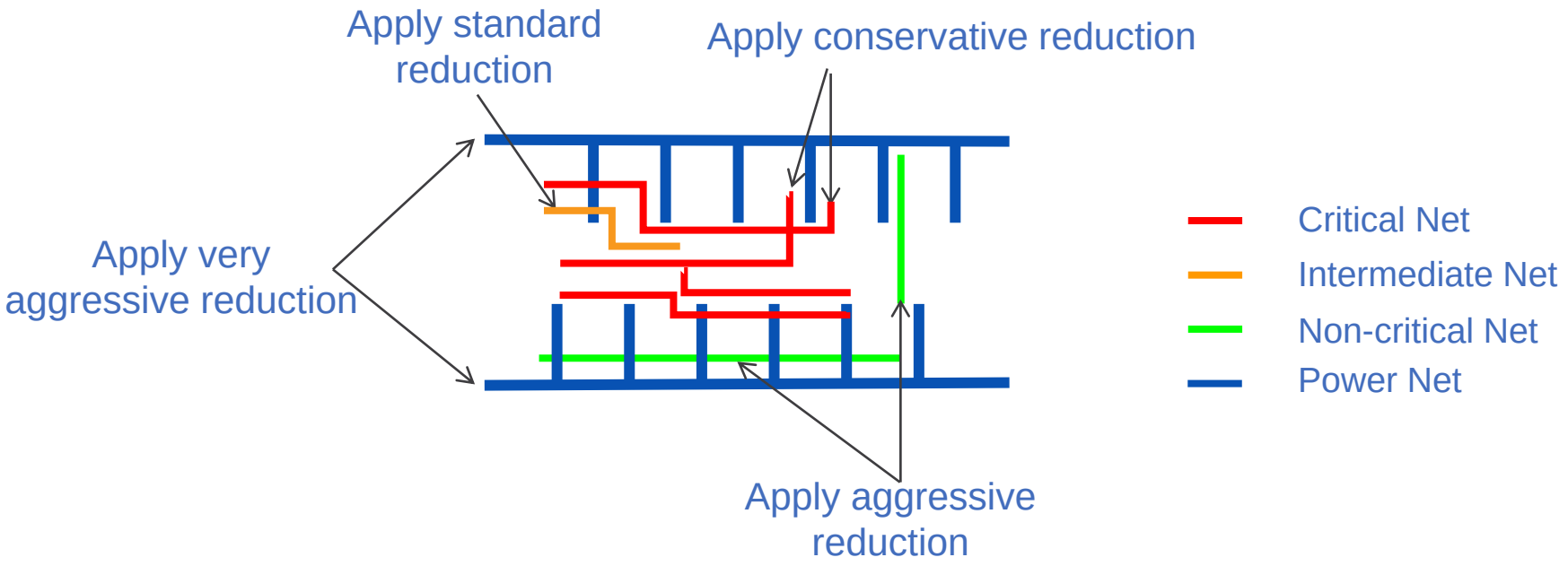
- Ideal for post-layout designs with long SPICE simulation times
  - Any Analog / Mixed-signal / RF block
- Examples:
  - ADC (Analog to Digital Converter)
  - AFE (Analog Front End)
  - DAC (Digital to Analog Converter)
  - PLL (Phase Locked Loop)
  - DLL (Delay Locked Loop)
  - VCO (Voltage-Controlled Oscillator)
  - CTLE (Continuous Time Linear Equalizer)
  - LDO (Low Dropout)

# Jivaro Deliver Superior SPICE Acceleration for All Tech. Nodes



# User Configurable or Auto Mode Reduction

- User customizable selective reduction
  - Apply different settings to different parts of the design. (Nets, paths or subckt's)
  - Accuracy parameters are customizable.
- Automatic selection with new Auto Mode

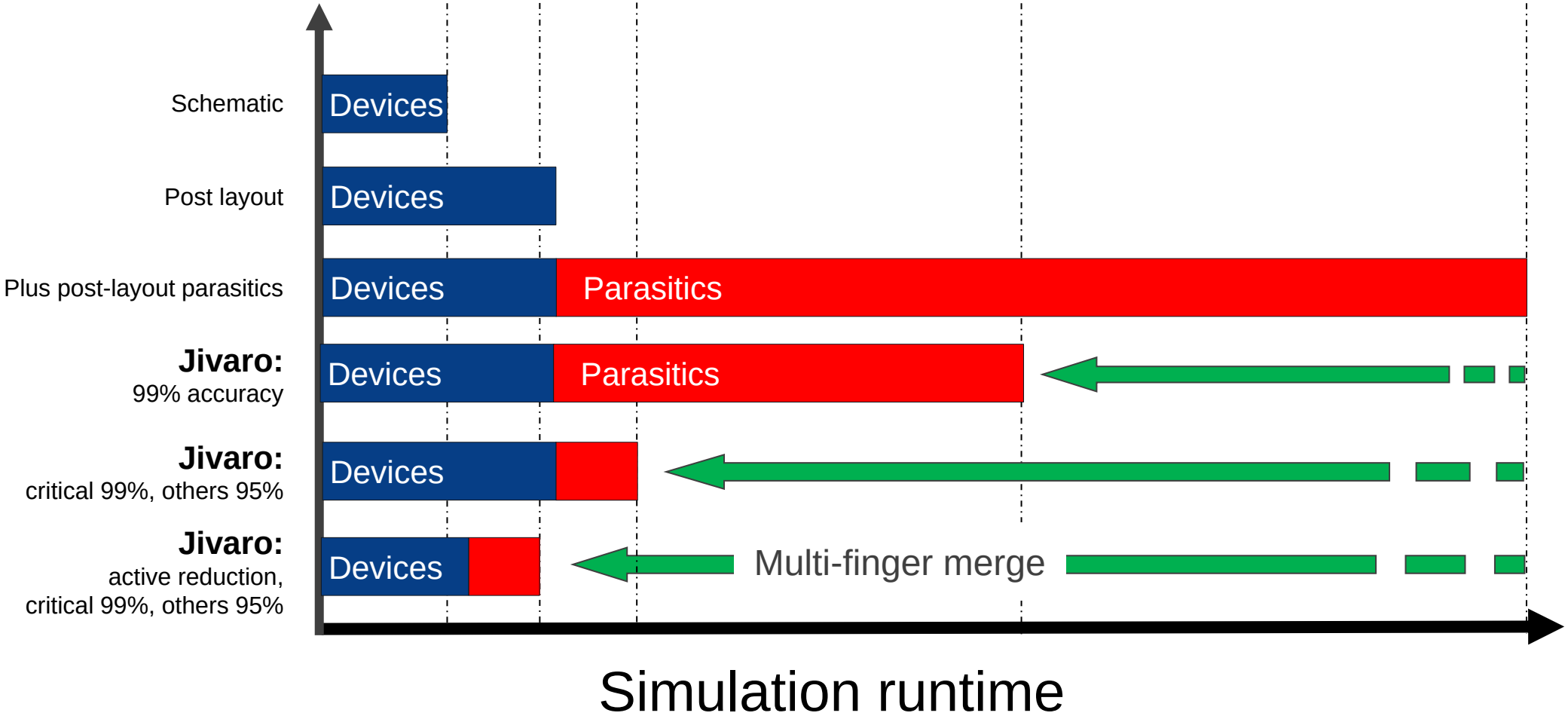


# Jivaro Advanced Features

## Multi-finger Merge

- Merging multi-finger devices speeds up simulation time while maintaining equivalent electrical behavior
- Possibility to detect and manage specific topologies
  - Semi dummy devices: three first pins connected to the same NET
  - Dummy devices: all pins connected to the same NET
  - Bypass devices: 1st and 3rd pins connected to the same NET
- Different methods of multi-fingers merge are available
  - Pins: merge of the pins only
  - Multiplier: merge of the devices without any update of the geometry parameters
  - Merge: merge of the devices with an update of the geometry parameters
  - Remove: device is deleted, and its pins are turned into internal nodes

# Jivaro Reduction Example



# Jivaro Automatic Reduction Mode

- Automatic Mode triggers advanced features to enable simplified usage
- Floating nets
  - Reduction of floating nets
- Devices
  - Merge of multi-finger devices
- Coupling caps
  - Decoupling of the coupling capacitances
- Power nets
  - Detection and selective reduction of power nets

# Summary

- 2-15X post-layout SPICE simulations speedup
- Maintain accuracy to <1%
- Enables running largest or impossible simulations
- Include power nets and metal fills in simulations for more accuracy
- Easy plug-n-play into existing flow using Auto Mode
- Customize the reduction to your objectives

Reliable

Powerful

Innovative

Flexible


Thank you
SILVACO