Role of i-aSi:H Layers in aSi:H/cSi Heterojunction Solar Cells

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***Abstract*—The dependence of solar cell parameters on i-aSi:H (non- or lightly-doped hydrogenated amorphous silicon) layer thickness in an aSi:H/cSi (crystalline silicon) heterojunction solar cell was analyzed using numerical simulation. By considering the quantum confinement effect at interfaces between i-aSi:H and cSi, experimental data which had not been explained by simulation could be successfully interpreted. The mechanism of an open-circuit voltage increase was visually presented by analyzing carrier distributions and quasi-Fermi levels near cSi surfaces and in the i-aSi:H layers. The optimized thicknesses of the i-aSi:H layers in both front and rear junctions were suggested to obtain the maximum conversion efficiency. The influences of the quantum confinement effect on the simulation results were discussed.**

***Index Terms*—Accumulation layer, conversion efficiency, crystalline silicon, fill factor, heterojunction, hydrogenated amorphous silicon, inversion layer, open-circuit voltage, quantum confinement, short-circuit current, solar cell.**

I. Introduction

Since the 1990s, aSi:H/cSi heterojunction solar cells have been widely studied [1], [2] as one type of high-efficiency cSi solar cells. It was experimentally reported that a majority carrier accumulation layer existed on the rear surface of cSi for the first time in 2006 [3] and that a minority carrier inversion layer was formed on the front (light receiving) surface of cSi in 2007 [4] and 2008 [5]. Recently Varache *et al*. extended above inversion layer analysis by introducing a quantum model to understand the inversion layer properties exactly and extract a band offset between aSi:H and cSi [6]. It has been experimentally demonstrated that the insertion of an i-aSi:H layer between the p-aSi:H layer (p-type aSi:H) and the cSi substrate improved the conversion efficiency (Eff) of the cell, especially the open-circuit voltage V_{oc} [7]. Recently, more detailed and advanced measured data on the effect of the i-aSi:H layer thickness were reported [8]. It is shown that V_{oc} increases and short-circuit current J_{sc} decreases with increased i-aSi:H layer thickness, and a maximum Eff exists in some intermediate i-aSi:H layer thickness (7 nm). However, the role of the i-aSi:H layer shown in the experiment has not yet been successfully explained in theory [9], [10]. The influence of the i-aSi:H layer thickness on the solar cell parameters has not been fully understood either.

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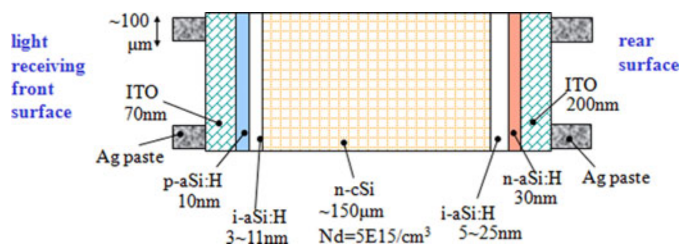

Fig. 1. Device structure of the solar cell.

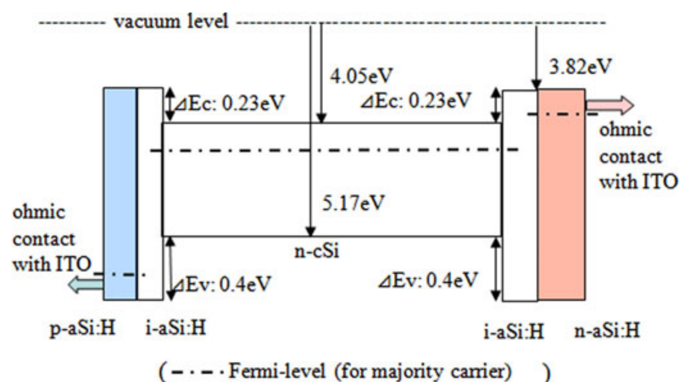

Fig. 2. Band diagram and energy levels used in the simulation.

In this study, a numerical simulation was carried out to study the influence of the i-aSi:H layer by using Silvaco's device simulator Atlas [11]. Band diagrams and carrier distributions of the front and rear junctions of the device were investigated in the device simulation. By considering the quantum confinement effect at the heterojunction interface, experimental data [8] were reproduced and explained successfully.

II. Simulation Structure, Parameters, and Models

The solar cell structure and band diagram used in the simulation are shown in Figs. 1 and 2, respectively. The device consists of a indium tin oxide (ITO)/p-aSi:H/i-aSi:H/n-cSi/i-aSi:H/n-aSi:H/ITO layer stack. The front ITO and p-aSi:H layer thicknesses were chosen to be 70 and 10 nm, respectively, to reduce unnecessary light absorption. Ohmic contacts between front ITO and p-aSi:H and between rear ITO and n-aSi:H were assumed to simplify the simulation. No textured surface for optical confinement was considered to simplify the calculation and

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TABLE I
PARAMETERS OF aSi:H USED IN THE SIMULATION, BANDGAP, DOPING, TAIL STATES, AND DEFECT STATE DISTRIBUTIONS

material		n-aSi:H	i-aSi:H	p-aSi:H
bandgap, Eg		1.75 eV	1.75 eV	1.75 eV
doping		1.51E19 cm^{-3} (phosphorus)	2.2E15 cm^{-3} (phosphorus)	2.05E19 cm^{-3} (boron)
conduction tail states	$N^{c\text{-}tail}_A$	1E21cm^{-3}	1E18 cm^{-3}	1E21cm^{-3}
	$E^{c\text{-}tail}_A$	0.07 eV	0.06 eV	0.07 eV
valence tail states	$N^{v\text{-}tail}_D$	1E21cm^{-3}	1E18cm^{-3}	1E21cm^{-3}
	$E^{v\text{-}tail}_D$	0.12 eV	0.09 eV	0.12 eV
acceptor-like dangling bond states	N^{db}_A	1E19 cm^{-3}	1E16 cm^{-3}	1E19 cm^{-3}
	E^{db}_A	0.7 eV	1.1 eV	1.3 eV
	δ^{db}_A	0.2 eV	0.15 eV	0.2 eV
donor-like dangling bond states	N^{db}_D	1E19 cm^{-3}	1E16 cm^{-3}	1E19 cm^{-3}
	E^{db}_D	0.45 eV	0.9 eV	1.1 eV
	δ^{db}_D	0.2 eV	0.15 eV	0.2 eV

Other than band gap, the same parameter values were used as in [9].

to focus on the fundamental role of the i-aSi:H. The thickness of cSi substrate was fixed to be 150 μm.

Bandgaps, doping concentrations, and distributions of tail states and defect-induced gap states in p-aSi:H, i-aSi:H, and n-aSi:H (n-type aSi:H) are listed in Table I, which were taken from [9]. The bandgap of aSi:H was set as 1.75 eV because the i-aSi:H may be deposited at a low temperature (lower than 200 °C) and with a high hydrogen content. Carrier mobility in the aSi:H films was set to be 5 cm^2/V/s for electrons and 1 cm^2/V/s for holes. Capture cross sections for donor-like and acceptor-like states were chosen as 10^{-16} and 10^{-14} cm^2, respectively. The surface recombination velocity of aSi:H was assumed as $v_{\mathrm{surf,n}} = v_{\mathrm{surf,p}} = 80$ cm/s. Minority carrier lifetime in the cSi was set to be 1 ms in a 1-Ω·cm n-cSi substrate. Other material parameters were default values in Atlas otherwise described.

A device coordinate was created in the device simulation. The x-axis was chosen to be parallel to all layer interfaces, while the y-axis was vertical to all layers. The Air Mass 1.5 global model was used as the solar insolation. Since we dealt with a 1-D problem, the transfer matrix method was used to analyze the optical paths through the device. Due to the high electric field at the energy barrier of the heterojunction, quantum confinement of carriers was considered by using a quantum potential model. In this model, an analytical expression of quantum potential obtained from the Schrödinger equation is added to the classical potential in the drift-diffusion equations. The quantum effect thus can be modeled without solving coupled classical transport equations and the Schrödinger equation. The models of thermionic emission and Fowler–Nordheim tunneling through the conduction or valence band barrier were used to describe the carrier transport across the heterojunction interface [12]. A thin (1 nm) defective cSi layer [13] was used at cSi substrate surfaces to model interface defects at the heterojunction with an interface defect density D_{it} of 10^{10}–10^{11} cm^{-2}. Both donor

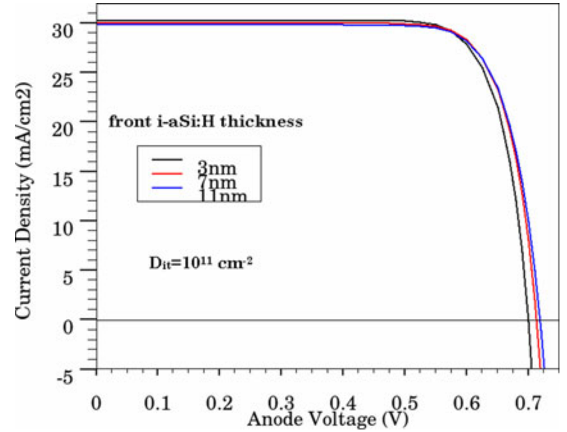

Fig. 3. *I–V* curves of cells with different i-aSi:H layer thickness.

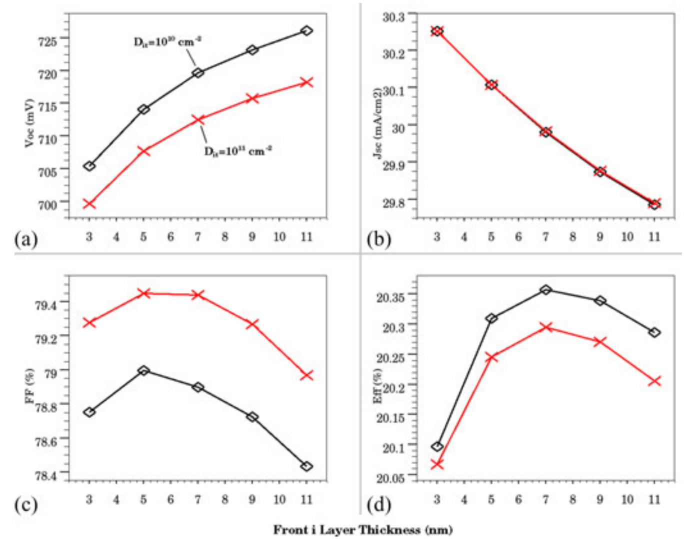

Fig. 4. Dependence of (a) V_{oc}, (b) J_{sc}, (c) FF, and (d) Eff on the front i-aSi:H layer thickness with two different D_{it}.

and acceptor capture cross sections for this layer were chosen as 10^{-16} cm^{-2}. The bandgap narrowing effect due to heavy doping was also taken into account.

III. Simulation Results

A. Influence of the Front Junction

Calculated *I–V* curves of the aSi:H/cSi solar cell are shown in Fig. 3 with different front i-aSi:H layer thicknesses in the front junction. The rear i-aSi:H layer is fixed at 7 nm. The difference in both V_{oc} and J_{sc} can be observed in the figure, whereas no difference in V_{oc} was recognized in [9]. Because of the back contact structure in [9], the optical path through the p-i-aSi:H/cSi junction is different from this paper and a weaker dependence of J_{sc} on the i-aSi:H layer thickness is expected. However, V_{oc} should exhibit some variation with the i-aSi:H layer thickness if the quantum model is included.

The dependences of V_{oc}, J_{sc}, fill factor (FF), and Eff on the front i-aSi:H layer thickness are shown in Fig. 4(a), (b), (c), and (d), respectively, with two different D_{it} values. We can see that

V_{oc} increases and J_{sc} decreases monotonically with increased i layer thickness, while FF and Eff reach their maximum values at some intermediate i layer thickness. The optimal value of the front i-aSi;H layer thickness at which the maximum efficiency is reached is around 7 nm. Such a dependence of the solar cell parameters on the i-aSi:H layer thickness is very similar to the experimental data [8]. With the variation of the i-aSi:H layer thickness from 5 to 10 nm in [8], V_{oc} increases from 691 to 712 mV, J_{sc} decreases from 35.5 to 35.0 mA/cm^2, FF shows relatively constant values up to 7 nm and decreases from 78.4 to 76.7%, and Eff reaches its maximum value 19.5% at the i-aSi:H layer thickness of 7 nm and decreases to 19.1%.

To investigate the mechanism of the cell parameters varying with the i layer thickness, the carrier concentration distribution and the band diagram and quasi-Fermi level (QFL) profile along the y-axis in the front junction region are shown in Fig. 5(a) and (b), respectively, for three different front i-aSi:H layer thicknesses under the open-circuit condition. We can see from Fig. 5(a) that holes pile up on the right side of the energy barrier in the front i-aSi:H/n-cSi junction, that is, a heavy inversion layer at the front surface of n-cSi is formed. This inversion layer was observed in the aforementioned experiments [4]–[6].

In the open circuit the minimum difference between electron QFL (E-QFL) and hole QFL (H-QFL) throughout the cell determines V_{oc}. As for our case, V_{oc} is equal to the voltage drop between E-QFL in the n-aSi:H and H-QFL in the p-aSi:H, as indicated in Fig. 5(b). The inset of Fig. 5(b) shows that an E-QFL offset, ΔE_{Fr}, at the rear cSi/i-aSi:H interface exists, caused by the quantum confinement effect. Since the geometry of the rear cSi/i-aSi:H junction is not changed in this case, ΔE_{Fr} is a constant and independent of the front i layer thickness. V_{oc} is hence linearly related to the difference between E-QFL in the cSi and H-QFL in the p-aSi:H. As the thickness of the front i-aSi:H layer increases, the electric field in the hole potential well at the front cSi surface becomes weaker, leading to weaker quantum confinement thus lower hole concentration in the well. As a result, the electron concentration increases accordingly, forcing E-QFL moving upward to the conduction band edge. Therefore, the separation of the H-QFL in the p-aSi:H and the E-QFL in the cSi increases, V_{oc} thus increases as well. Such a process can be observed by comparing the cases with the front i layer thickness equal to 3, 7, and 11 nm in Fig. 5.

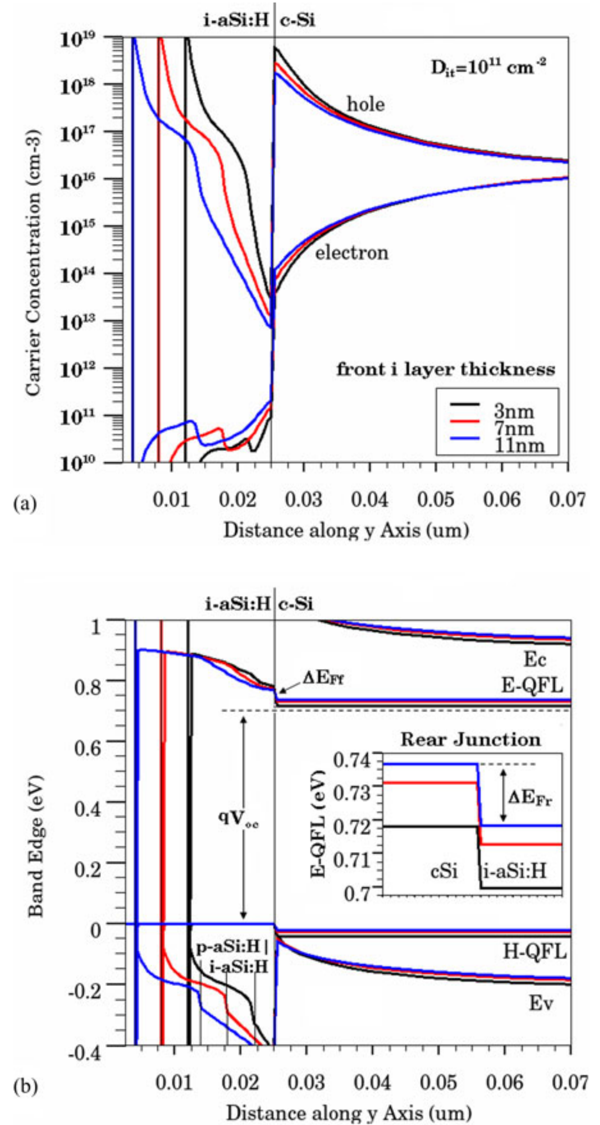

Fig. 5. (a) Carrier concentration distribution and (b) band diagram and quasi-Fermi level profile along y-axis in the front junction region with three different front i layer thicknesses under the open-circuit condition. The inset of Fig. 5(b) is the zoom-in view of the electron quasi Fermi level profile in the rear cSi/i-aSi:H junction with three different front i layer thicknesses.

B. Influence of the Rear Junction

The dependences of V_{oc}, J_{sc}, FF, and Eff on the i-aSi:H layer thickness in the rear junction are shown in Fig. 6(a), (b), (c), and (d), respectively, in cases of three different front i-aSi:H layer thicknesses. The variation of the cell parameters on the rear i layer thickness is somewhat different from that in Fig. 4. J_{sc} decreases and FF increases monotonically with the increased rear i layer thickness, while V_{oc} and Eff reach their maximum values at some intermediate i layer thickness. The maximum V_{oc} appears at the rear i-aSi:H layer thickness of 11–13 nm and the optimal value of the rear i-aSi;H layer thickness for the maximum efficiency is around 19–21 nm. The difference suggests that the mechanism associated with the rear i layer thickness will differ from that related to the front i layer thickness.

Fig. 7(a), (b), and (c) shows, respectively, the carrier concentration distribution, electric current density and the band diagram, and QFL profile along the y-axis in the rear junction region with three different rear i-aSi:H layer thicknesses under the open-circuit condition. The front i-aSi:H layer is fixed at 7 nm. Photo-generated carriers arrive at the rear junction by diffusion. Electrons accumulate at the rear cSi surface as was experimentally observed [3], while holes are pushed away by the back surface field (BSF), leaving a much lower density. As the rear i layer thickness increases, the BSF decreases, hole current density thence increases, as shown in Fig. 7(b). Note that both drift and diffusion components of the hole current decrease simultaneously here. Since these two components are

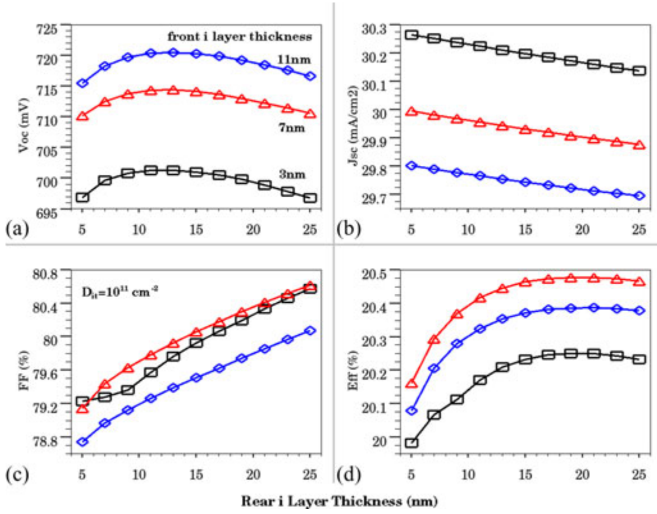

Fig. 6. Dependence of (a) $V_{\rm oc}$, (b) $J_{\rm sc}$, (c) FF, and (d) Eff on the rear i-aSi:H layer thickness in cases of three different front i-aSi:H layer thicknesses.

in the opposite direction in the open circuit, the net effect is that the total hole current increases with the increased rear i-aSi:H layer thickness. In order to maintain the zero current in cSi, the E-QFL offset at the front i-aSi:H/cSi interface [ΔE_{Ff}, as shown in Fig. 5(b)] increases to allow more electrons being emitted through the front junction to compensate the increased hole current density. On the other hand, weaker BSF leads to weaker quantum confinement of electrons at the rear cSi surface; the E-QFL offset at the rear cSi/i-aSi:H interface (ΔE_{Fr}) is thus smaller. The inset of Fig. 7(c) shows the E-QFL profile near the rear cSi/i-aSi:H junction for three different rear i-aSi:H layer thicknesses. The positions of E-QFLs on the cSi side are mainly determined by ΔE_{Ff} and those in the rear i-aSi:H layer are determined by $\Delta E_{Ff} + \Delta E_{Fr}$. Since $V_{\rm oc}$ is proportional to the separation between E-QFL in the n-aSi:H and H-QFL in the p-aSi:H, it increases first with the increased rear i layer thickness due to weaker quantum confinement at the rear junction and then decreases as a result of the stronger electron emission at the front junction.

Fig. 6(b) shows that $J_{\rm sc}$ decreases slowly with the increase of the i-aSi:H layer thickness. This is because the short-wavelength portion of the incident light is mainly absorbed in the front aSi:H layers and little reaches the rear i-aSi:H layer. The overall effect of the rear i-aSi:H layer on $V_{\rm oc}$, $J_{\rm sc}$, and FF results in a maximum value of efficiency at some intermediate i-aSi:H layer thickness.

IV. Discussions

A. Influence of the Quantum Confinement Effect

For the case without the quantum model, the dependences of $V_{\rm oc}$, $J_{\rm sc}$, FF, and Eff on the front i-aSi:H layer thickness are shown in Fig. 8(a), (b), (c), and (d), respectively, with two different $D_{\rm it}$ values. The rear i-aSi:H layer is fixed at 7 nm. We can see that $V_{\rm oc}$ almost does not change with the i-aSi:H layer thickness and Eff decreases with the increased i layer thickness

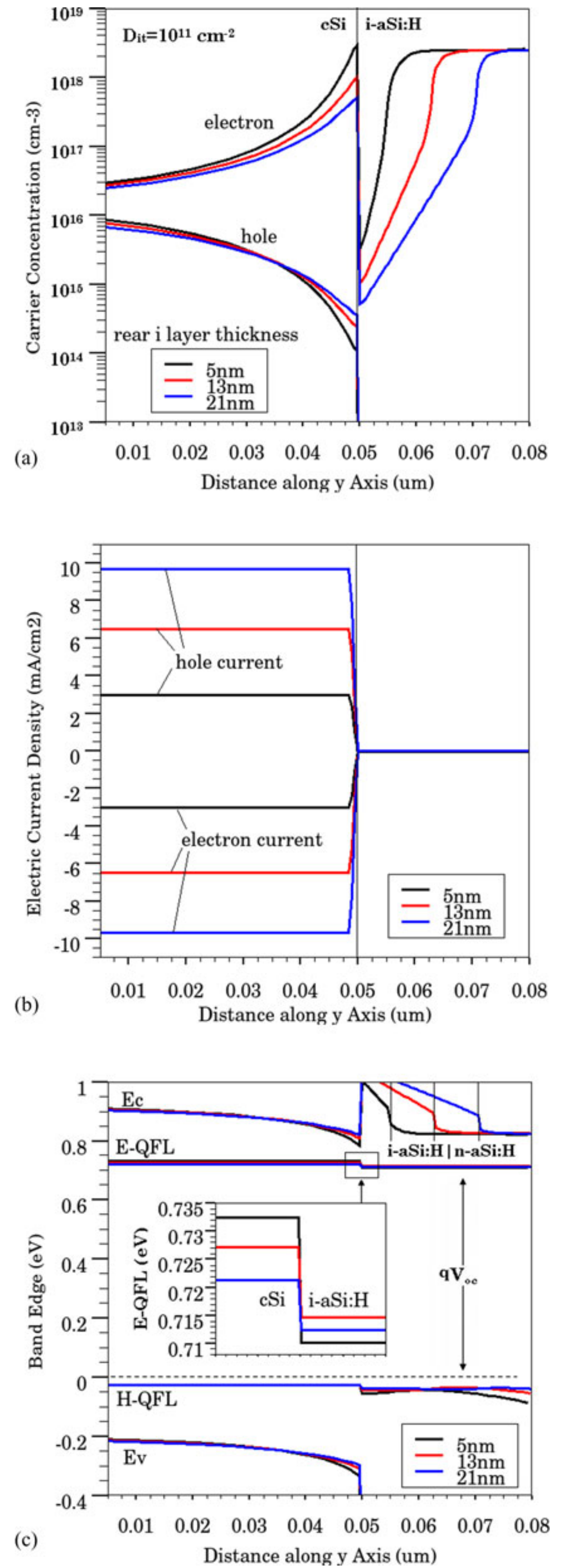

Fig. 7. (a) Carrier concentration distribution, (b) electron and hole electric current density distribution and (c) band diagram and quasi Fermi level profile along y-axis in the rear junction region with three different rear i-layer thicknesses under the open-circuit condition. The inset of Fig. 7 (c) is the zoom-in view of the electron quasi-Fermi level profile in the rear cSi/i-aSi:H junction with three different rear i-layer thicknesses.

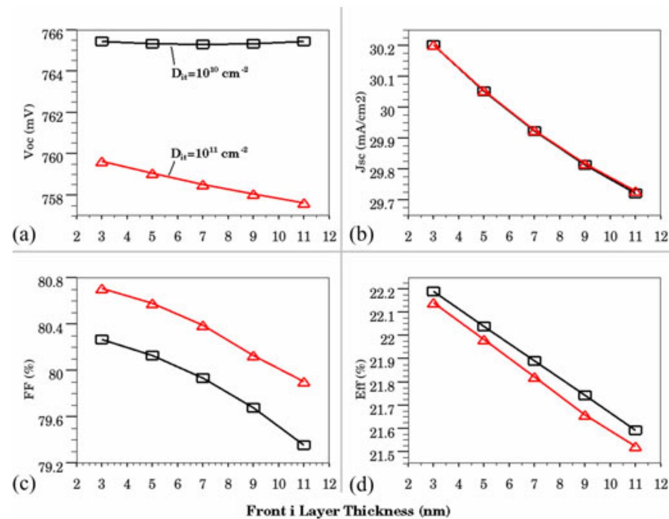

Fig. 8 Dependence of (a) $V_{\rm oc}$, (b) $J_{\rm sc}$, (c) FF, and (d) Eff on the front i-aSi:H layer thickness with two different $D_{\rm it}$. The quantum model is excluded.

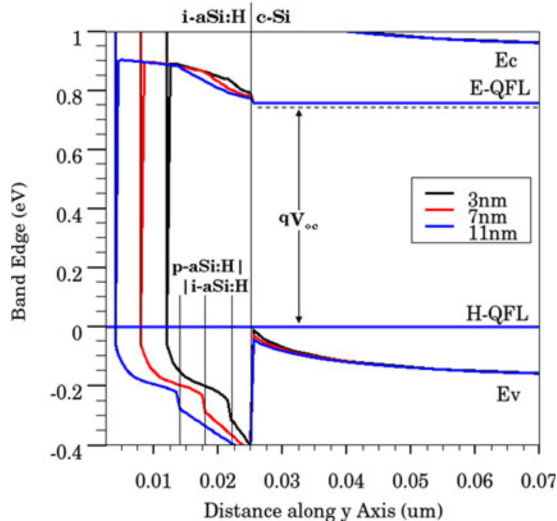

Fig. 9. Band diagram and quasi Fermi level profile along y-axis in the front junction region with three different front i layer thicknesses under the open-circuit condition. The quantum model is excluded.

monotonically. The dependences of $V_{\rm oc}$ and Eff on the i layer thickness are almost the same as those in [9] and [10], but do not coincide with experimental results [8]. We can also see from Fig. 8(a) that the value of $V_{\rm oc}$ is much larger than the measured data ($\sim$10% larger), leading to an overestimating of the efficiency.

The key difference between cases with and without the quantum model is the different QFL separation, which determines the $V_{\rm oc}$. Fig. 9 shows the band diagram and QFL profile along the y-axis in the front junction region without the quantum model under the open-circuit condition. The split in both E-QFL and H-QFL for different front i-aSi:H layer thicknesses does not appear here, unlike the quantized case in Fig. 5(b). $V_{\rm oc}$ is thus independent of the i layer thickness as indicated in Fig. 9. Because of the strong valence band bending and hole inversion at the front cSi surface, it is not reasonable to ignore the quantum

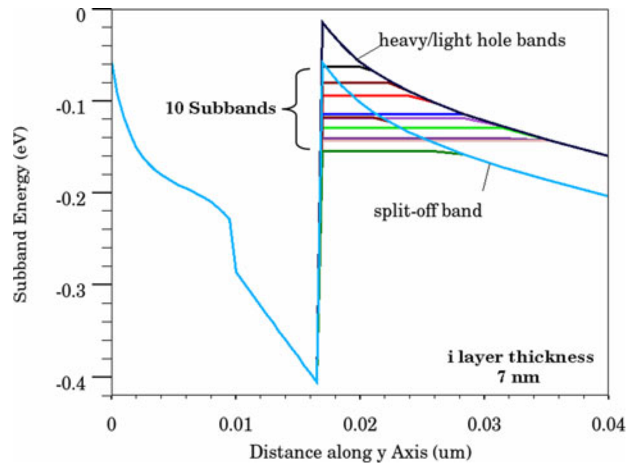

Fig. 10. Lowest ten subband energy levels in the hole well of the front cSi surface. Subband energy levels were obtained by solving self-consistently the Poisson–Schrödinger equations.

confinement effect in this region. Fig. 10 shows the lowest ten subband energy levels in the hole potential well of the front cSi surface. Results were obtained by solving self-consistently the Poisson–Schrödinger equations using Atlas [11]. We can see that the lowest four subbands are well separated with each other and the lowest subband level is 48 meV ($\sim$1.8 kT) away from the valence band edge. Without the quantum model, the same forward current density will be obtained at a higher forward bias, resulting in a larger $V_{\rm oc}$. These make it evident that the quantization effect is notable; it is thus necessary to use quantum models in the simulation to correctly understand the device physics.

B. *Value of the Short-Circuit Current*

$J_{\rm sc}$ in our simulation is about 30 mA/cm^2, which is smaller than the experimental counterpart [8]. The main reason is that no textured cSi surface was used in the simulation. The textured front surface serves as a light-trapping structure and has been widely adopted in the modern silicon solar cell technology to improve $J_{\rm sc}$. Experimentally measured $J_{\rm sc}$ in textured cells usually has a value of 35–39 mA/cm^2 [1], [2], [8], [14]. On the other hand, the highest $J_{\rm sc}$ in the solar cell without the textured surface (planar cell) has been reported to be 32 mA/cm^2 so far [14]. Another reason is that the thickness of the cSi substrate in the simulation is only 150 μm, half of most cases. Our simulation shows that $J_{\rm sc}$ is increased by 1 mA/cm^2 in a cell with a 300-μm cSi substrate due to the increased length of the optical path in the cSi. Therefore, our best simulated $J_{\rm sc}$ (31.3 mA/cm^2) is very close to the best experimental value (32 mA/cm^2) in the planar cell. Although the textured structure affects the optical path in the cell and $J_{\rm sc}$ a little, it does not change the layer profile much and our analyses on the i-layer thickness dependence of the cell parameters are still meaningful.

C. *Influence of the Interface Defect Density*

Fig. 11 shows the cell parameter dependence on the interface defect density $D_{\rm it}$. We can see that the cell parameters are not

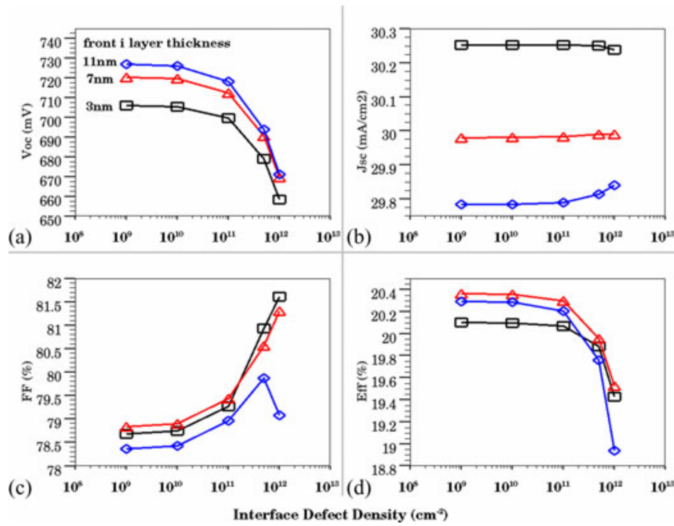

Fig. 11. Dependence of (a) Voc, (b) Jsc, (c) FF, and (d) Eff on the Dit at front junction in cases of three different front i-aSi:H layer thicknesses. The rear i-aSi:H layer is fixed at 7 nm.

affected a lot by the interface defect when $D_{\rm it}$ is less than 10^{11} cm^{-2}, especially for $J_{\rm sc}$ and Eff. However, $V_{\rm oc}$ and Eff drop dramatically as $D_{\rm it}$ is increased from 10^{11} to 10^{12} cm^{-2}. Therefore, it is necessary to control $D_{\rm it}$ far less than 10^{12} cm^{-2} to maintain high efficiency. Since the origin of the interface defect is ascribed to the imperfect passivation of the cSi surface by i-aSi:H, it is crucial to improve the passivation quality of i-aSi:H on the cSi to realize a low $D_{\rm it}$. In the present simulation, a hypothetical thin damaged layer at the front cSi surface with a constant defect density [13] was used to mimic the situation.

D. Material Parameter Variation in Device Fabrication

In the present simulation, the material properties of the i-aSi:H layer are supposed to be uniform throughout the layer. This is a good approximation for the study on the role of the i-aSi:H layer thickness in the device physics. However, it was reported that the content of di-hydride and the structural defect density is larger during the initial growth of i-aSi:H on cSi [15], [16], but the defect may be reconstructed during the further growth of the i-aSi:H. As a result, the actual value of $D_{\rm it}$ varies with the i-aSi:H thickness for the initial few nanometers and then becomes constant for a thicker i-aSi:H layer (e.g. thicker than 4 nm). The carrier recombination rate at the i-aSi:H/cSi interface will vary as well. For a few nanometers of i-aSi:H on top of the cSi substrate surface different material parameters should be used for a more accurate simulation.

The surface recombination of photogenerated carriers largely depends on the process equipment, process environment, and process condition, for example, the post-deposition annealing temperature [17] of aSi:H. The carrier mobility of aSi:H is also dependent on the condition of the deposition process. If a deposition process leads to a smaller carrier mobility, then the optimum value of the i-aSi:H layer thickness will be smaller. Therefore, the accurate extraction of parameters like $D_{\rm it}$ from experimental data is necessary for an exact fitting of the simulated characteristics to the experimental characteristics.

V. Conclusion

The influence of the i-aSi:H layer at both front and rear junctions of an a-Si:H/cSi solar cell was investigated using numerical simulation. The mechanisms of the i-aSi:H layer thickness dependence of device parameters—$V_{\rm oc}$, $J_{\rm sc}$, FF, and Eff—were visually presented by analyzing the carrier distribution and QFL profile at the front and rear surface of cSi and in aSi:H layers. By considering the quantum confinement effect at i-aSi:H/cSi interfaces, the experimentally reported result of $V_{\rm oc}$ increasing with increased i-aSi:H layer thickness was successfully explained. The optimum values of the i-aSi:H layer thickness are suggested to be 6–8 nm for the front junction and 19–21 nm for the rear junction, at which the maximum conversion efficiency of 20.5% can be achieved in a nontextured cell.

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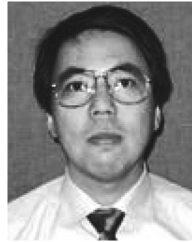

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