Enabling Netlist Driven Layout with Standard Cells

Introduction

Netlist Driven Layout (NDL) using Gateway and Expert provides a powerful tool for streamlining the process of creating IC layout from a schematic. The pcell libraries provided in the Silvaco PDKs contain device layouts that match individual devices in the schematic, and these PCells are set up to be used in the NDL flow. However, many designs use customer created standard cell layouts that correspond to subcircuits in a schematic. These layout cells would need to be modified and included in the NDL flow in order to pass the net information from the schematic to the layout.

A simple example using logic cells is provided below to illustrate the steps required to enable NDL capabilities into standard cell layouts. In the example used below, the layout of an inverter, NAND, and NOR gate has been created, and the process of enabling NDL capabilities for these standard cells is described.

Gateway NDL Setup

After the underlying transistors are placed and wired together in the schematic for the logic subcircuits, symbols can be created by using the symbol auto-generation feature by selecting Tools->Generate Symbol, or creating a new symbol by selecting File->New->Symbol. Once symbols are created for the 3 logic gates, an NDL string must be created to pass the net information from the schematic to the layout using the NDL netlist.

With the inverter symbol open, select Edit->Properties to bring up the symbol property editor window. A property called “PREFIX” is then added with a value of “X” to be used in the NDL netlist to define the element as a subcircuit, and a property called “NAME” will hold the subcircuit identifier, in the case of the inverter it will be listed as “inv”. The syntax of the NDL netlist entry for this symbol is determined by the NDL string, which is set by clicking on the NDL button in the Properties window. The NDL string should be entered to pass the instance prefix, instance number, pin list, and instance name as shown in Figure 1.

Figure 1. Symbol Property Editing and NDL String.

The same procedure is followed for the NOR and NAND gate symbols. More detailed information about symbol properties and netlist string editing can be found in the Gateway User’s Manual.

Once the circuit with the logic symbols is complete, the NDL netlist can be generated from Gateway by selecting Simulation->View NDL Netlist.

Map File and Include File

Before the Gateway NDL netlist can be loaded into the Expert layout tool, two files need to be created that map the instances in the netlist to layout cells in Expert. The first file is a .map file that maps the subcircuit instance name in the netlist to the layout database containing the cell that the subcircuit represents. The syntax is as follows:

```
inv  logic_cells::inv
nand2       logic_cells::nand2
nor2 logic_cells::nor2
```

The first column contains the subcircuit name from the schematic and the second column contains the layout database name (logic_cells) and the layout cell name.

The second file is the include file which defines the pin information for each subcircuit or device that is used in NDL.

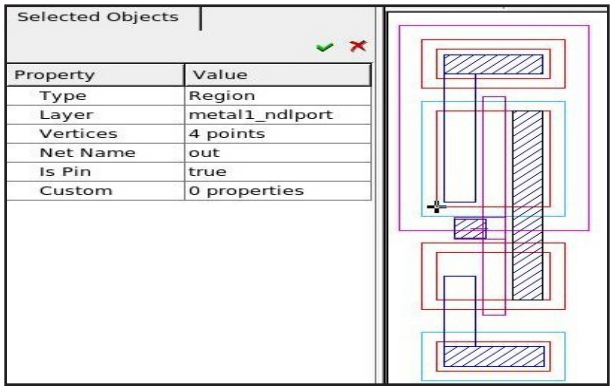

Figure 2. Property Window for Inverter Layout Cell 'out' Port.

The syntax is provided below:

```
*.SUBCKT_DEV inv 4
*.SUBCKT_DEV nand2 5
*.SUBCKT_DEV nor2 5
.subckt inv in out vdd vss
.ends
.subckt nand2 in1 in2 out vdd vss
.ends
.subckt nor2 in1 in2 out vdd vss
.ends
```

The pin information above will map the nets in the NDL netlist to the layout ports based on the pin order and pin names. The include file is automatically loaded when the map file is selected by having both file handles have the same name, for instance, logic_cells.inc and logic_cells.map in this example.

Adding Ports to the Layout

In order to pass the net information to the standard cell layout, ports must be added to each of the example logic cells that match the pin names used in the include file.

Using the NDL port layers supplied with the Silvaco PDK techfile, shapes are drawn over each part of the layout that will serve as a port. Then select each shape and edit the properties to include the net name and change the "Is Pin" property to "true". If no NDL port layers are present in the techfile, they will need to be created and set up to have proper layer connectivity with the underlying routing layer.

Loading the NDL netlist

After each of the standard cells has been modified to include the correct ports, the NDL netlist can be loaded by selecting Tools->Netlist Driven Layout->Load Netlist, and browsing to the NDL netlist that was created in Gateway. An undefined subcircuit warning will initially appear since the map file has not been loaded. From the Netlist Editor window, select File->Load Map and browse to the map

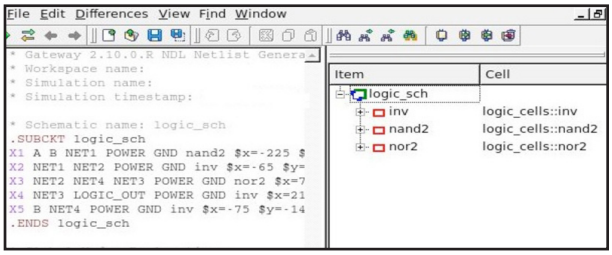

Figure 3.Netlist Editor Window.

file. Then select File->Reload for the cell mapping and the include file to take effect. The top level circuit name and hierarchy will appear in the netlist rover on the right hand side of the Netlist Editor window as shown in Figure 3.

If the cell mapping was successful then each instance in the top level circuit will show the layout library and cell name it is mapped to as shown in Figure 3.

To create the layout, right click on the top level circuit name in the netlist rover and select "Create". Layout instances of the standard cells will then be placed in a newly created cell matching the name of the top level circuit in the NDL netlist. Then the layout instances will contain the netlist information necessary to use the Expert features designed to aid in routing. Figure 4 below shows two of the inverter standard cells with the electrical connections visible using the net flight-line feature.

Conclusion

Using the NDL flow in Gateway and Expert can greatly simplify the process of creating IC layout from a schematic by automatically transferring net information, proper device types and sizes, and subcircuit hierarchy. The addition of enabling standard cells to use NDL shares those advantages, providing the layout designer with many tools in Expert to produce a finished layout in less time and with less chance for routing errors. The steps outlined above can be applied to any customer created standard cell layout that has an analogous subcircuit or device in the circuit schematic.

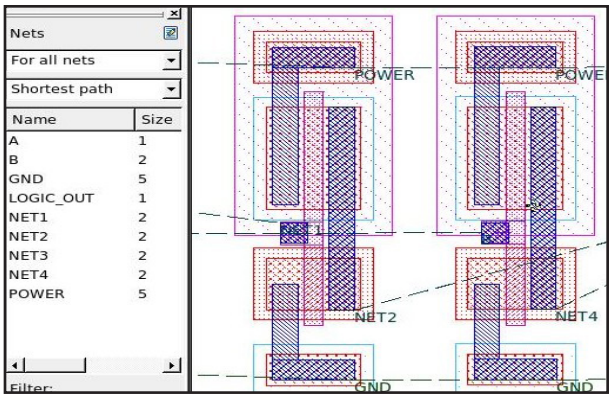

Figure 4. Layout Instances Showing Net Flight-Lines.