Selective RC-extraction Methods in Guardian LPE for Post-layout Circuit Simulations

Introduction

Shrinking geometries and increased design complexity have added greater chip functionality, but have also reduced the predictability of modeling at device level. For example, to accurately model the behavior of a transistor, the number of parameters has grown significantly beyond simple length and width. Silvaco Guardian LPE extracts source and drain attributes, well proximity and STI stress effect parameters, that are essential in nanometer scale designs. Interconnect parasitic effects can cause an entire chip to fail, and must be correctly accounted for in post-layout simulation and analysis to ensure acceptable yield. Hipex RC coupled with Guardian LPE extracts interconnect parasitic resistance and capacitance.

The number of extracted RC elements is usually huge. Various reduction algorithms in Hipex RC can considerably reduce this number, but it may be still too big to simulate full chip design with all RC elements using SPICE simulator. A practical way to reduce RC parasitic element count is to identify areas where parasitic effects are important to account for and extract RCs only for these areas. A careful selection can maintain RC count sufficiently low as to permit reasonable SPICE simulation time. This Application Note describes two different methods of selective RC extraction: critical cell extraction and critical nets parasitic extraction.

I. Design and Setup Requirements

To perform specific post-RC simulations after the LVS validation of the circuit, it is necessary to follow some rules from the beginning to the end of the design process. These rules are especially related to the consistency between the circuit layout description (designed with Expert Layout Editor) and circuit schematic description (made by Gateway Schematic Editor). The better this consistency is, the easier it will be for the designer to include specific RC elements coming from the LPE extraction in the schematic to perform a correct post-RC simulation of the circuit.

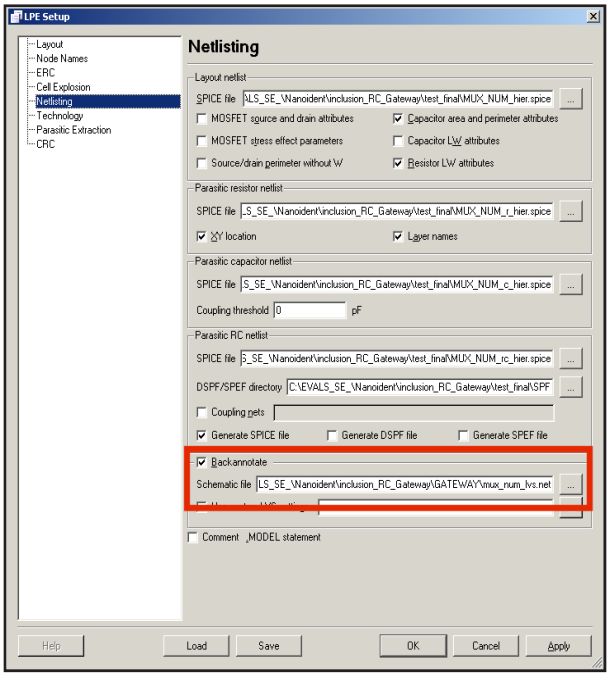

Figure 1. Back-annotation activation.

Cells definition:

This is the first important aspect of the consistency between schematic view and layout view of the circuit. As much as possible, it is advised to have correspondence between the hierarchical structures of the schematic and the layout. It means that each subcircuit in the schematic should represent a cell on the layout. Moreover, this rule is useful for the processing of the “Netlist Driven Layout” function and for the LVS validation step.

Back-annotation activation:

Generally it is better that the name of a node on the layout is consistent with the name of the corresponding node on the schematic. If this rule cannot be followed, use the back-annotation function of Guardian LPE.

This way, the netlist being generated by Guardian LPE will have full coherence with the netlist describing the schematic concerning the node names. The back-annotation function can be activated in the “Netlisting” panel of the Guardian LPE setup windows (menu: “Verification >> Extraction >>Setup” in Expert Layout Editor GUI or Guardian LPE GUI)

In Figure 1 the back-annotation is activated referring to the schematic netlist “mux_num_lvs.net”. All node names of this netlist will be automatically propagated to matching nodes of the netlist extracted from the layout.

Cell ports definition:

Cell ports are layout objects defining the Inputs and Outputs (I/Os) of cells. Consequently they will have direct impact on the I/Os of the sub-circuits (“.SUBCKT” terms) in the netlist generated by the LPE tool. This characteristic of several aspects in the goal of a successful post-RC simulation be taken care of:

- It is strongly advised to define these ports as labels (i.e. text objects) on the layout. The names of the ports will be consistent with symbols I/Os of the schematic
- These labels must be designed using layers which are configured to automatically generate some ports. To do this, select “Setup >> Technology >> Layer Connection Setup” from the Guardian LPE “Layer Connection setup” panel. The highlighted option in Figure 2. (see below) has to be activated. With this setup all labels created with layer “Met1_Text” will generate a port

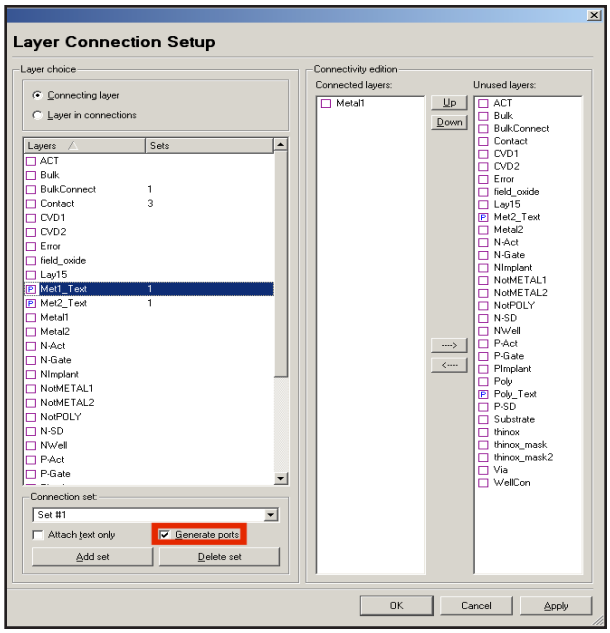

Figure 2. Configuration of the ports generation.

- To get proper RC distribution inside the cell port labels should be placed in the locations where the net connects to other cells in the design hierarchy

These ports will represent the physical and electrical bounds of the cell and of the sub-circuit representing this cell in the extracted netlist.

Global nodes:

This is a significant difference that usually exists between a netlist extracted from a layout and a schematic description. Most of the time, the schematic contains lots of implicit node connections across the hierarchy. This is not the case on the layout: this one requires physical connections only.

These nodes will be sub-circuit ports in the netlist extracted from the layout by Guardian LPE but not in the schematic description. They should only be removed by the user in the list of ports in the netlist of the extracted cells. The parasitic elements found on these nodes will be taken into account during the post-RC simulation.

II. Methods of Selective RC Extraction

As mentioned in the introduction, it is convenient to know which are the regions of the layout being sensitive to RC elements. From this knowledge two kinds of methods of selective parasitic extraction can be used.

Selective parasitic extraction “by cell”:

If the user identifies cells of the layout containing critical RC elements only the corresponding cells with Hipex RC engine of Guardian LPE can be extracted if the user chooses.

Note: It is very important to extract each critical cell as top cell. In this way, all the RC parasitic elements of these cells will be included in the netlist. This result can be obtained if the user selects each desired cell as the top cell in the “Layout” panel of Guardian LPE setup and then launches a parasitic extraction for each one.

In order to launch the RC parasitic extraction use the “Verification >> Extraction >> Hipex RC >> Run” menu in Expert Layout Editor or Guardian LPE.

If all design requirements have been followed the user will be able to include these files in the Gateway schematic netlist. Consequently, this netlist will contain the deck of simulation (stimuli, analyses, and model cards) and the rest of the circuit description. This will result in a ready-to-use netlist for post-RC simulation with SmartSpice.

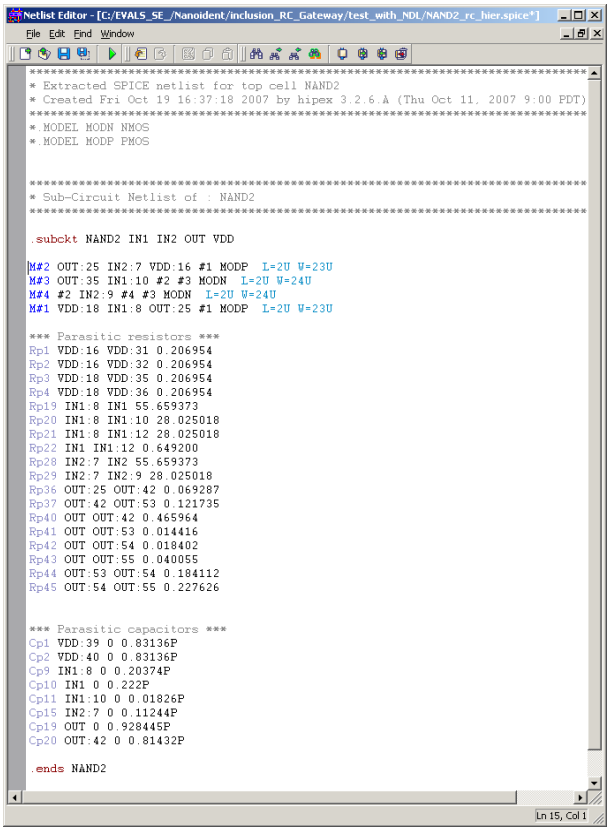

Figure3. Netlist of a cell obtained with Guardian LPE (including RC elements).

In Figure 3, a specific cell “NAND2” has been extracted from a whole project by following the design requirements described above. This netlist contains all physical devices and RC parasitic elements extracted by Guardian LPE. This netlist is ready to be included in a schematic netlist as replacement of the subcircuit “NAND2” of this netlist. In this way the SPICE simulation of this netlist will take into account any parasitic element of cell “NAND2”.

Notes:

- It is important to take care of the pins order’s consistency between the schematic netlist sub-circuits calls and the Guardian LPE netlist sub-circuits
- A useful option for a direct use of the netlist is the “Comment .MODEL statement” option. It can be activated in the “Netlisting” panel of Guardian LPE setup window

This method of selective RC extraction “by cell” can be useful if the designer wants to perform post-RC simulations concerning various regions of the layout.

Selective parasitic extraction “by net collection”:

If some critical nets of the layout are known, a dedicated function of Guardian LPE can be directly used to extract only the RC elements attached to these nets. This function can be activated in the “Parasitic Extraction” panel of Guardian LPE setup window.

The user can define lists of nets to be extracted, or alternatively some lists of nets to be ignored during the parasitic netlist extraction.

For example, in the Guardian LPE configuration shown in Figure 4, a collection of nets called: “nets_to_extract” has been defined. This collection contains nets “IN”, “OUT” and “CLK”. The “selected nets” box is checked: this means that only these 3 nets will be concerned by parasitic extraction.

This method of selective RC extraction “by net collection” will not necessarily require that all design requirements described above be followed. This can be a convenient alternative to the first method of selective extraction “by cell”. Selective net extraction results in faster run times and less memory consumption than full RC extraction only if number of selected nets is significantly smaller than total number of nets in the design.

Conclusion

Hipex RC and Guardian LPE allow the user to accurately and efficiently capture the nanometer effects and RC parasitics for accurate post-layout SPICE simulation. Two methods of selective RC-extraction described in this Application Note enable to get high accuracy modeling parameter extraction and interconnect parasitic extraction for sensitive circuits and nets, and still enable full SPICE simulation to give designers greater confidence in their post-layout verification.

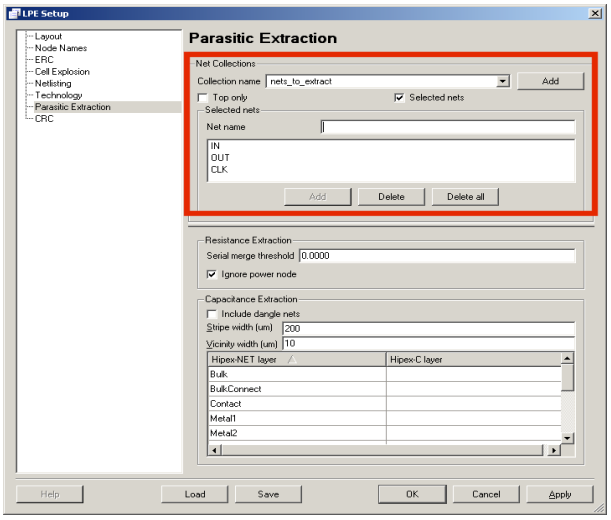

Figure4. Setup of the selective net extraction in Guardian LPE.