# Hipex RC: 7 Techniques for Reducing a RC Netlist

## Introduction

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Hipex RC is accurate and fast full-chip hierarchical extraction software that performs extraction of parasitic capacitances and resistances from hierarchical layouts. Parasitic RC netlists are sometimes too large to run post-layout simulation. Hipex RC provides several methods to reduce large RC netlists, and this application note introduces seven techniques for doing so.

#### 1. Merge series resistances

Select "Parasitic Extraction" in "Layout Parameter Extraction Setup" window, and enter "Serial merge threshold (Ohm)" value of "Resistance Extraction" (Figure 1). A resistance, which is below a given threshold, merges with the biggest resistance next to it (Figure 2).

This is effective for eliminating the many small resistances that can be generated in long distance interconnects with many corners.

	Layout Param	eter Extraction Setup	
Layout	Parasitic Extraction	1	
-Node Names			
- ERC	- Net Collections		
- Cell Explosion	Collection name default		
- Netlisting	Conection name   deladic		Add
- Technology	F Top only F Se	elected nets F BA names	Incremental CDB, RDB
Parasitic Extraction	_ Ignored nets		
CRC	Net name		
<ul> <li>Backannotation and LVS</li> </ul>			
	Capacitance Extraction	Add Delete Delete all	I
	Scripe width (um) 200		
	Vicinity width (um) 10		
	Hipex-NET layer 🗸	Hipex-C layer	-
	CONTACT		_
	DEEP_N_WELL		
	GC_port		
	M2_LABEL		
	M3_LABEL		
	M4_LABEL		-1
	INSTART		_
	Resistance Extraction		
	Serial merge threshold (Ohm	) 1	F Ignore power node
	RC Reduction     Scattering Parameter Mac     Time Domain Reduction	romodels Time threshold (sec)	
Help	Specify number of processo	rs (Parallel Mode): 2 2 (Max=2)	Cancel Apply

Figure 1. Serial merge threshold setup.



Figure 2. Effect of merging resistances by 10hm.

### 2. Merge coupling capacitances into ground capacitances

Select "Netlisting" in "Layout Parameter Extraction Setup window", and enter "Coupling threshold" value of "Parasitic capacitor netlist" (Figure 3).

Hipex RC does not report coupling capacitances below this threshold. Instead, it contributes them to the ground capacitances of the two coupling (Figure 4).

This is effective if small coupling capacitances can be ignored.

	Layout Parameter Extraction Setup			
Layout	Netlisting			
-Node Names	_ Layout netlist			
Cell Explosion	SPICE file limucad analog demo(1.1.4.8/expert/examples/quickstart/App. completed hier spice			
Netlisting	gence me imucau analog demort 1.1.4. Avex per dexamples/quicks tardxpp_completed_menspice			
- Technology - Parasitic Extraction - CRC - Backannotation and LVS	I MOSFET LW attributes only			
	□ Source/drain gerimeter without W □ Capacitor L <u>W</u> attributes			
	Resistor LW attributes			
	Parasitic resistor netlist			
	SPICE file mucad-analog-demo/1.1.4.R/expert/examples/guickstart/App_completed_r_hier.spice			
	로 Y location 모 Layer names			
	Parasitic capacitor netlist			
	SBIGE tile mucad analeg.deme/1.1.4.B/expertienamples/quickstart/App.completed.c.hier.spice			
	Coupling threshold 1			
	cooping difestion 1 pr			
	Parasitic RC hetiist			
	SPICE file pucad-analog-demo/1.1.4.R/expert/examples/quickstart/App_completed_rc_hier.spice			
	DSPF/SPEF directory /PDK/demo/simucad-analog-demo/1.1.4.R/expert/examples/guickstart/SPF			
	- Distribution mode			
	C Thrifty C Accurate			
	Coupling mode			
	C Selected nets			
	Ignored nets			
	Generate SPICE file     Generate DSPF file     Generate SPEF file     Generate SPEF file			
	Comment MODEL, .END statements T Output parasitic net models T Comment top .subo			
	Netlist line length 80			

Figure 3. Coupling threshold setup.

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Figure 4. Effect of merging capacitances by 1pF.



Figure 6. Effect of disabling coupling capacitances.

#### 3. Disable coupling capacitances mode

Select "Netlisting" in "Layout Parameter Extraction Setup window", and disable "Coupling mode" of "Parasitic RC netlist" (Figure 5).

Hipex RC does not report all coupling capacitances. Instead, it contributes them to the ground capacitances.

This is effective if the effect of all coupling capacitances can be ignored.

-Layout	Netlisting		
-ERC	Layout netlist		
Cell Explosion	SPICE file mo/simucad-analog-demo/1.1.4.R/expert/examples/quickstart/res_merge_hier.spice		
-Netlisting -Technology -Parasitic Extraction	MOSFET LW attributes only     Capacitor area and perimeter attributes     Source/drain perimeter without W     Capacitor LW attributes		
- CRC - Backannotation and LVS			
backarmotation and Evo	Parasitic resistor netlist		
	SPICE file no/simucad-analog-demo/1.1.4.R/expert/examples/guickstart/res merge r hier.spice .		
	ע צץ location ע Layer names		
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	SPICE file ho/simucad-analog-demo/1.1.4.R/expert/examples/quickstart/res_merge_c_hier.spice		
	cooping circulate pr		
	Parasitic RC netlist SPICE file o/simucad-analog-demo/1.1.4.R/expert/examples/quickstart/res_merge_rc_hier.spice		
	DSPF/SPEF directory /PDK/demo/simucad-analog-demo/1.1.4.R/expert/examples/quickstart/SPF		
	C Distribution mode C Thrifty C Accurate		
	C Coupling mode		
	C Selected nets		
	© Ignored nets		
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	Comment "MODELEND statements T Output parasitic net models T Comment top .subcl		
	Netlist line length 80		
Help	Load Save OK Cancel Apply		

Figure 5. Disable coupling mode.

#### 4. Selective cells and nets

Hipex RC can extract only selected cells and nets. This method is described in detail in another application note, "Selective RC-extraction Methods in Guardian LPE for Post-layout Circuit Simulations".

This is effective if you know in advance which cells and nets are critical for the circuit.

# 5. Thrifty mode

Select "Netlisting" in "Layout Parameter Extraction Setup window", and select "Thrifty" under "Distribution mode" (Figure 7).

Node Names	I suggit patilist		
RC	Layout hetiist		
ell Explosion	SPICE file imucad-analog-demo/1.1.4.R/expert/examples/quickstart/App_completed_hier.spice		
Technology	☐ MOSFET LW attributes only ☐ Capacitor area and perimeter attributes		
Parasitic Extraction	□ Source/drain perimeter without W □ Capacitor LW attributes		
CRC Backannotation and LVS	Resistor LW attributes		
	←Parasitic resistor netlist		
	SPICE file mucad-analog-demo/1 1.4.8/expert/examples/quickstart/App.completed r hier spice		
	Ir <u>Layer</u> names		
	Parasitic capacitor netlist		
	SPICE file mucad-analog-demo/1.1.4.R/expert/examples/quickstart/App_completed_c_hier.spice		
	Coupling threshold 0 pF		
	Parasitic BC netlist		
	EDICE file used apples demoit 1.4 Dispertieuromoles/ausisterant/tep completed as hier spice		
	SPICE life locad-analog-demo/1.1.4.k/experdexamples/duckstart/xpp_completed_ic_lifer.spice		
	DSPF/SPEF directory /PDK/demo/simucad-analog-demo/1.1.4.R/expert/examples/quickstart/SPF		
	Distribution mode		
	C Accurate		
	P Coupling mode		
	C Calendaria		
	C Ispected nets		
	i ignored nets		
	In Generate SPICE file In Generate DSPF file In Generate SPEF file		
	♥ Comment "MODEL, .END statements   Output parasitic net models   Comment top .sub		
	Mattine line to all the		
	Nedisc line length 180		

Figure 7. Select Thrifty mode.

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Figure 8. Effect of thrifty mode.

In thrifty mode, Hipex RC extracts only a capacitance per couple of nodes. As shown in Figure 8, there are three capacitances between "A" node and "B" node. These capacitances are reduced to one capacitance by thrifty mode.

This is effective if accuracy of relative positions for interconnects is not necessary.

#### 6. Built-in RC Reduction

Select "Parasitic Extraction" in the "Layout Parameter Extraction Setup window", and enable "RC Reduction" (Figure 9). Hipex RC uses two techniques for the builtin RC reduction. The first one is based on the Scattering Parameter Macromodeling method. The second one is based on the time constant reduction method.

	Layout Paran	ieter Extraction Setup	
- Layout	<b>Parasitic Extraction</b>	ı	
Node Names			
ERC	- Net Collections		
-Cell Explosion	Collection name default		Add
Netlisting	concentor nume   denoted		
Technology	T Top only T S	elected nets F BA names	Incremental CDB, RDB
Parasitic Extraction	Ignored nets		
CRC Deckensetation and LVC	Net name		
		Add Delete Delete all	]
	Capacitance Extraction		
	I Include dangle nets		
	Stripe width (um) 200		
	Vicinity width (um) 10		
	Hipex-NET layer 🗸	Hipex-C layer	<u> </u>
	CONTACT		
	DEEP_N_WELL		
	GC_port		
	M2_LABEL		
	M2_LABEL M3_LABEL		
	M2_LABEL M3_LABEL M4_LABEL		
	M2_LABEL M3_LABEL M4_LABEL M5_LARFI		
	M2_LABEL M3_LABEL M4_LABEL M5_LABEL Resistance Extraction		
	M2_LABEL M3_LABEL M4_LABEL M5 LABEL Resistance Extraction Serial merge threshold (Ohn	n) [100	 ✓ Ignore power node
	M2_LABEL M3_LABEL M4_LABEL M4_LABEL M4_LABEL Serial merge threshold (Ohn	0) 100	▼ Ignore power node
	M2_LABEL M3_LABEL M4_LABEL M5_LABEL Resistance Extraction Serial merge threshold (Ohn	1) [100	▼ F Ignore power node
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	M2_LABEL       M3_LABEL       M4_LABEL       M4_LABEL       JM5 i ARFI       Serial merge threshold (Ohn       IF RC Reduction       G Scattering Parameter Mac       C Time Domain Reduction	n) 100 romodels I'me threshold (sec) 0	⊻ ⊽ Ignore power node
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	M2_LABEL       M3_LABEL       M4_LABEL       M4_LABEL       M6_LABEL       M6_LABEL       M6_LABEL       M6_CRC       M6_CRC       Cr       Time Donain Reduction       Cr       Specify number of processs	n) 100 romodels Time threshold (sec) 0 ors (Parallel Mode): 2 🚊 (Max=2)	⊻ Ø Ignore power node

Figure 9. RC Reduction setup.

Both methods eliminate a node in a parasitic net with a small RC value by distributing this value to neighborhood nodes.

For more detailed information refer to section 4.5 "RC Reduction in HipexNetlister" in the Hipex User's Manual.

#### 7. RC Reduction using ClarityRLC

Select "CRC" in "Layout Parameter Extraction Setup window", and set up the options in this window (Figure 10).

Using this reduction method, ClarityRLC is executed from Expert's menu after Hipex RC execution. Clarity-RLC is a powerful reduction tool and has several options for reducing RLC netlists.

For more detailed information refer to the ClarityRLC User's Manual.

	Layout Parameter Exclaction Setup	
- Layout - Node Names	CRC	
- ERC	_ Input/Output	
Cell Explosion	Format SPICE	
- Technology	Input file ad-analog-demo(1.1.4.R/expert/examples/quickstart/App.completed.rc.bier.spic	
- Parasitic Extraction	Output file on 0.1.4 Discussion production of Control o	
CRC	Output me po/1.1.4.R/expert/examples/quickstart/CRC_Files/App_completed_rc_nier.spice.crc	
Backannotation and LVS	Reduction	
	✓ Authorize reference node     ✓ Parallel check	
	Port File	
	Details	
	☐ Title Line	
	E Detailed display	
	, becareo grapio y	
	Ground nodes Ports Thresholds Ignore	
	Thresholds	
	Resistance Threshold for All Colls	
	Capacitance Threshold for All Cells 1e-15	
	Resistance Threshold for Unnamed Top Cell	
	Capacitance Threshold for Unnamed Top Cell	
	Cell 🗸 Resistance Capacitance	
	1 App_completec	
	2 error_amp_com 3 ido completed	
	4 silvaco_demo_	
	OK Cancel	
Help	Load Save OK Cancel Appl	

Figure 10. ClarityRLC setup.

### Conclusion

Hipex RC has enough options to reduce RC netlists. Users can select which combinations are best according to the target circuits. ClarityRLC can efficiently and accurately reduce linear parasitic RLC elements in parasitic extracted netlist. Using these techniques, users can reduce parasitic capacitances and resistances thus significantly reducing runtime of post-layout simulations.