

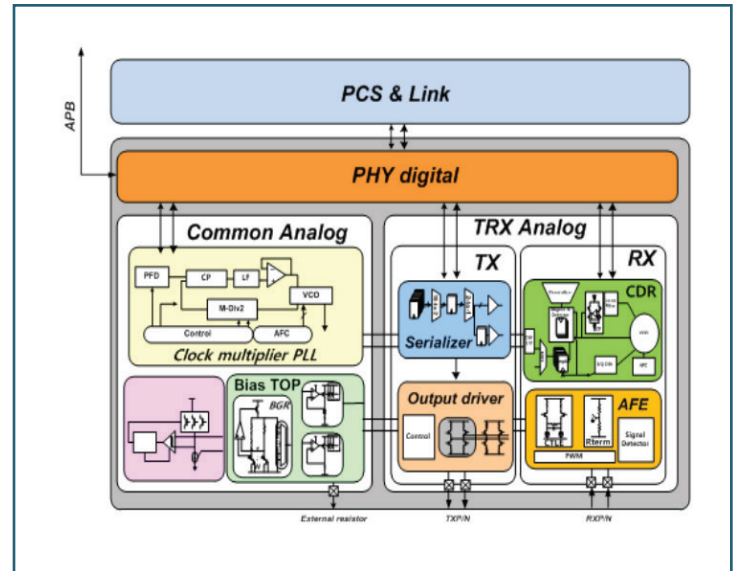
## PCIe PHY n-Lane

### Overview

The PCIe PHY is a hard macro PHY for the PCIe protocol. IO pads and ESD structures are included with extensive built-in self test features such as loopback and scan support. It offers a cost-effective and low-power solution. It builds on silicon-proven designs that are in volume production.

### Key Features

- 8nm low power CMOS device technology
- 1.8V, 0.85V dual power supply
- Compliant to PCIe Base 4.0 specification
- Support Gen1, Gen2, Gen3, and Gen4
- Channel configuration for data lanes
  - o Common (CMN) and 1/2/4 data lanes
- Support the following pre-emphasis levels
  - o - 3.5/-6dB for Gen1/2
  - o 3-tap FIR with resolution of 1/36 for Gen3 and Gen4
- 100MHz reference clock is required
- Support 100MHz differential clock I/O
- Built-in self test feature capable of producing and checking PRBS random patterns



### Deliverables

- Front-end DK : Timing LIB, Verilog model, sample test bench
- Back-end DK : Physical view LEF, GDSII layout, DRC, LVS
- Documentation : Datasheet and user guide

# SAMSUNG Foundry

For more information, please contact us at [IP@silvaco.com](mailto:IP@silvaco.com).

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