

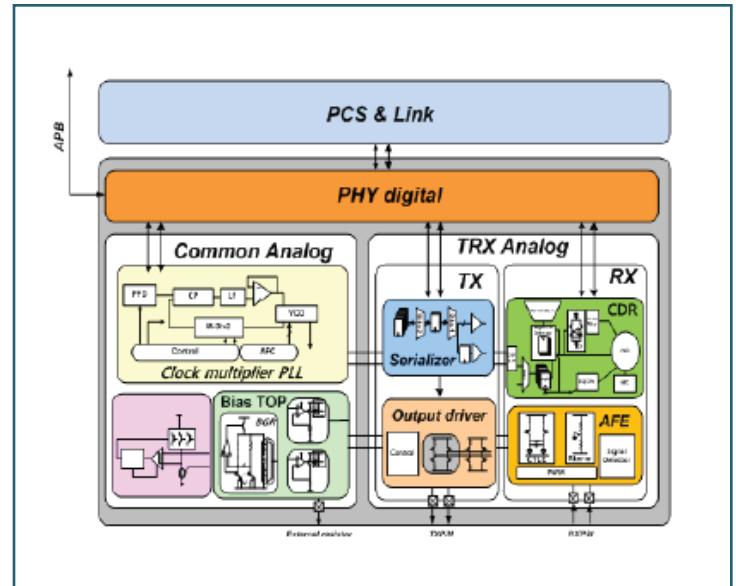
USB/DisplayPort TX PHY

Overview

This is a hardmacro PHY for the USB3.1 and DP TX protocols. IO pads and ESD structures are included with extensive built-in self test features such as loopback and scan support. It offers a cost-effective and low-power solution. It builds on silicon-proven designs that are in volume production.

Key Features

- Samsung Foundry 10nm low power CMOS device technology
- 1.8V, 0.85V dual power supply
- Compliant to USB 3.1 (SS only), DP V1.4 (TX only), and DP Alt Mode specification
- Supports USB3.1 Gen1, Gen2, and DP TX RBR, HBR2, HBR3
- 3-tap Tx FIR with resolution of 1/36
- Decision Feedback Equalization and CTLE
- 26MHz reference clock is required
- Supports Spread Spectrum Clocking (up to -0.5% supported)
- Built-in self test capable of producing and checking PRBS random patterns



Deliverables

- Front-end DK: Timing LIB, Verilog model, sample test bench
- Back-end DK: Physical view LEF, GDSII layout, DRC, LVS
- Documentation: Datasheet and user guide

SAMSUNG Foundry

For more information, please contact us at IP@silvaco.com.

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