

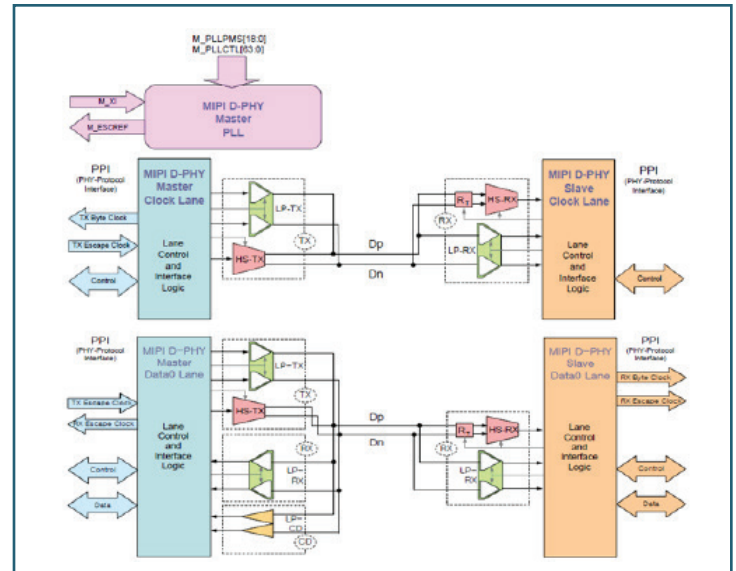
MIPI D-PHY/C-PHY Combo PHY

Overview

The Samsung Foundry MIPI D-PHY/C-PHY combo PHY IP is a hard macro PHY for CSI RX and DSI TX. IO pads and ESD structures are included with extensive built-in self test features such as loopback and scan support. It offers a cost-effective and low-power solution.

Key Features

- 10nm low power CMOS device technology
- 1.8V, 0.85V, 1.2V power supply
- Compliant to D-PHY V2.0 and C-PHY V1.1 specification
- Lane configuration
 - o 4.5Gbps D-PHY Master 4 lanes for DSI TX
 - o 2.5Gbps C-PHY Master 3 trios for DSI TX
 - o 4.5Gbps D-PHY Slave 4 lanes for CSI RX
 - o 2.5Gbps C-PHY Slave 3 trios for CSI RX
- Global operation timing parameters control
- Backward compatible with previous versions
- Built-in self-test feature capable of producing and checking PRBS random patterns



Deliverables

- Front-end DK: Timing LIB, Verilog model, sample test bench
- Back-end DK: Physical view LEF, GDSII layout, DRC, LVS
- Documentation: Datasheet and user guide

Applications

- Mobile / IoT

SAMSUNG Foundry

For more information, please contact us at IP@silvaco.com.

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Rev 012720_02
71300