

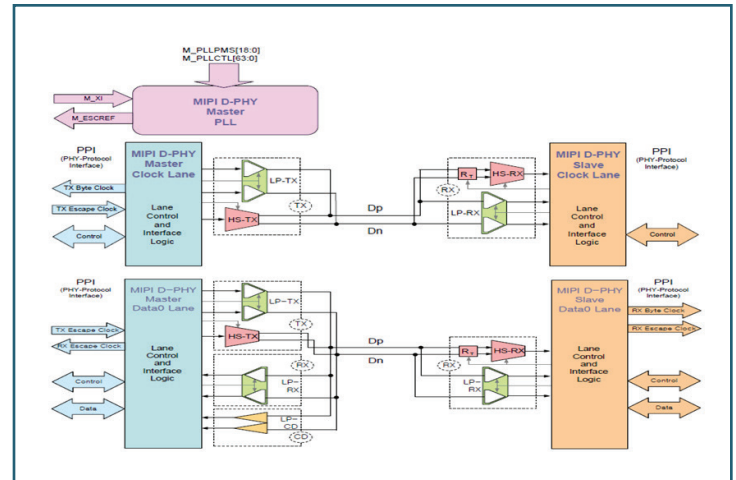
## MIPI D-PHY

### OVERVIEW

The MIPI D-PHY IP is a hardmacro for a CSI RX and DSI TX. IO pads and ESD structures are included with extensive built-in self test features such as loopback and scan support. It offers a cost-effective and low-power solution. The MIPI D-PHY builds on silicon-proven designs that are in volume production.

### KEY FEATURES

- Samsung Foundry 14nm low power CMOS device technology
- 1.8V, 0.9V, 1.2V power supply
- Compliant to D-PHY V1.2 specification
- Lane configuration
  - o 2.1Gbps D-PHY Master 4 lanes for DSI TX
  - o 2.1Gbps D-PHY Slave 4 lanes for CSI RX
- Global Operation Timing Parameters Control
- Backward Compatible with previous versions
- Built-in self test feature capable of producing and checking PRBS random patterns



### DELIVERABLES

- Front-end: Timing LIB, Verilog model, Sample test bench
- Back-end: Physical view LEF, GDSII layout, DRC, LVS
- Documentation : Datasheet and User's guide

# SAMSUNG Foundry

For more information, please contact us at [IP@silvaco.com](mailto:IP@silvaco.com).

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