

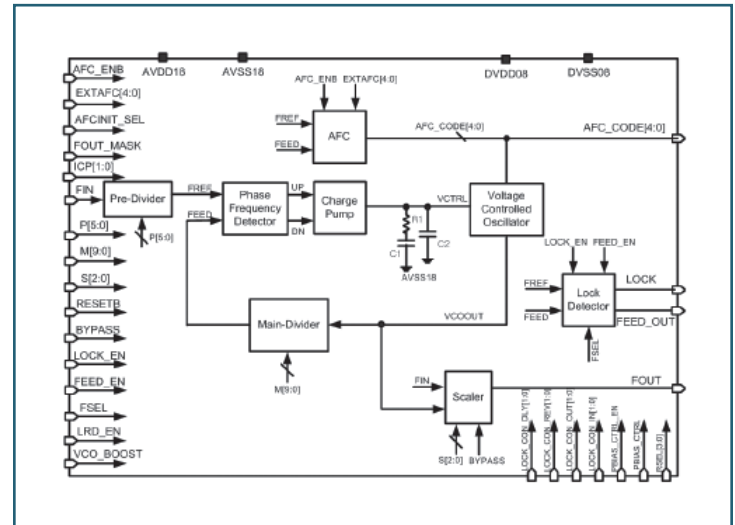
2.0GHz Integer PLL

Overview

This is a dual supply voltage integer Phase Locked Loop (PLL). It generates an output clock which is determined by a 6-bit pre-divider, 10-bit main-divider and 3-bit scaler. The input clock bypass mode, lock detection and glitch-free function are available.

Key Features

- 14nm Low Power CMOS device technology
- 1.8V, 0.9V to 0.8V dual power supply
- Operation junction temperature (T_j): -40 to 125°C
- Input frequency range: 4MHz to 300MHz
- Output frequency range: 32MHz to 2.0GHz
- Period Jitter: $\pm 1.5\%$ of VCO clock period
- Output clock duty ratio: 47 to 53%
- Glitch-free scaler / Input bypass mode ($F_{OUT} = F_{IN}$)



Deliverables

- Datasheet
- User Guide
- Verilog model
- Timing DK
- CDL netlist
- Layout (GDS2 or OAS)

Target Applications

- Mobile/Consumer

SAMSUNG Foundry

For more information, please contact us at IP@silvaco.com.

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Rev 062619

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