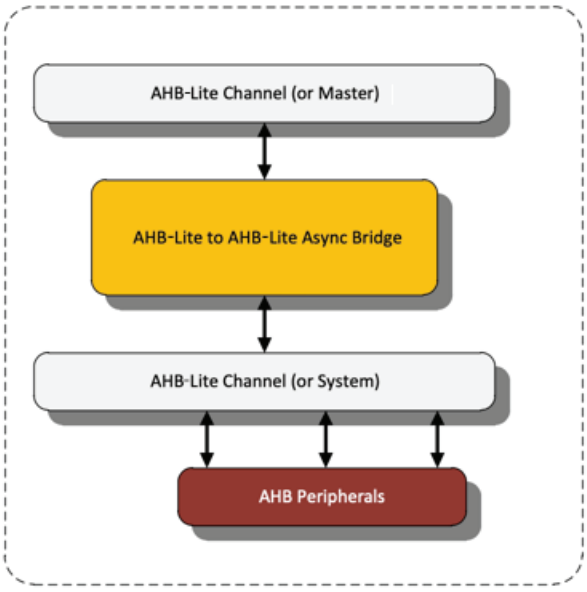
AHB-Lite to AHB-Lite Asynchronous Bridge

DESCRIPTION

The AHB-Lite to AHB-Lite Asynchronous Bridge translates an AHB-Lite bus transaction (read or write) on one clock domain to an AHB-Lite bus transaction on a second (asynchronous) clock domain. This allows two completely independent AHB-Lite systems to communicate and share data. The bridge is implemented as two state machines - one on the initial or "A" domain and another on the secondary or "B" domain, and several synchronizers. The AHB-Lite to AHB-Lite Asynchronous Bridge acts as an AHB-Lite Slave on the "A" domain, and an AHB-Lite Master on the "B" domain.



FEATURES

- Translates AMBA® AHB-Lite transactions to AMBA® AHB-Lite transactions
- Interfaces two totally asynchronous AHB-Lite domains
- Supports any ratio of relative clock frequencies
- Low Gate Count
- Conforms to AHB-Lite signaling rules

Deliverables

- Verilog Source
- Complete Test Environment
- AHB Bus Functional Model
- C-Sample Code

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