

AXI Performance Subsystem – ARM A5

The **AXI Performance Subsystem** is an AMBA® AXI4 based system that is useful as the digital infrastructure for building SOCs needing high performance. This system contains an **8 master, 16 slave AXI4 multi-matrix** for supporting multiple high speed user AXI masters while providing high performance with Cortex-A5 class processors.

Additionally, the subsystem includes two DMA controllers for easily moving data from user peripherals to the “interleaved” internal SRAM controller for the highest contiguous SRAM performance possible.

Closely coupled Instruction and Data SRAM are available to the CPU as independent AXI multi-matrix slaves with high priority.

The **AXI Performance Subsystem** includes a standard set of peripherals and cores that supports RTOS and software kernels. Included is a QSPI, serial flash controller for boot loading program images or operating as an Execute in Place (XIP) engine using non-volatile external flash memory with low power.

The **AXI Performance Subsystem** is soft IP that can be used in all the popular semiconductor technology nodes.

TARGET APPLICATIONS

- Gateways / Routers
 - Automotive, IoT, Wireless
- Medical
 - Instrumentation / Display
- Home / Office
 - Surveillance / Monitoring / Home Automation
- Industrial
 - System Controllers, Analysis
- Avionics / Military
 - Displays, Communications

FEATURES

- High Performance
- Linux Support
- RTOS/Kernel Support
- AMBA AXI4 Multi-layer Fabric
- AMAB APB 3.0
- Internal Interleaved SRAM Controller
- QSPI Serial Flash Controller
- Standard APB Peripherals

PROCESSOR OPTIONS

- ARM Cortex-A5

INFRASTRUCTURE

- AXI4 Multi-layer Fabric
- 8 Masters – 16 Slaves
- APB 3.0 Bus Channel / Decode
- AXI to APB Bridge (3)

IP CORES

- Power Management Unit
- 8, 16, 32-bit Internal SRAM Controller
- Internal Interleaved SRAM Controller
- DMA Controller (2)
- QSPI Serial Flash Controller with Execute in Place (XIP)
- Standard Peripherals
 - Watchdog Timer, Timers (2), GPIO
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- Configurable
 - I2C Master, SPI Master / Slave, 16550 UART

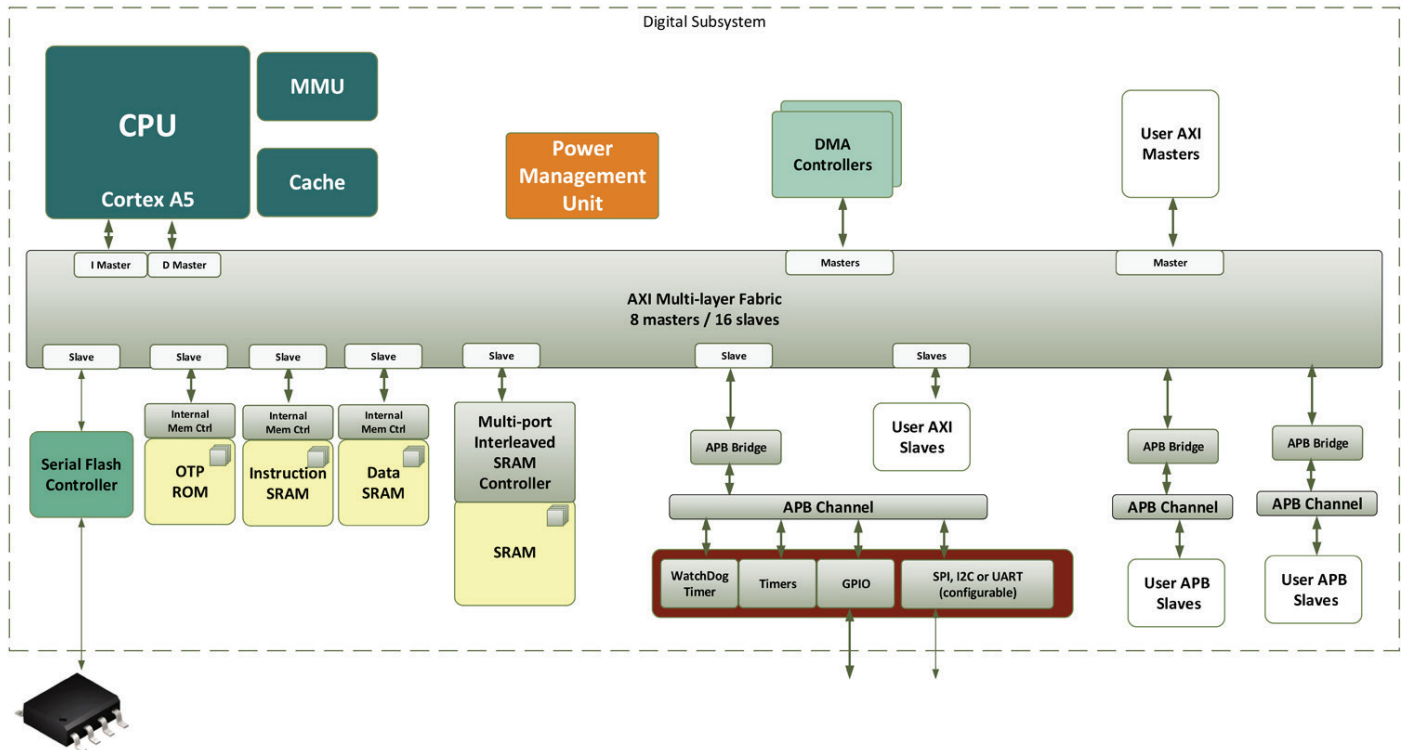
SOFTWARE

- RTOS (Free RTOS)
- Embedded Linux
- Flash Loader, Boot Loader
- Interrupt Handlers
- Hardware Adaption Layer / Drivers
 - SPI, I2C, GPIO, QSPI, DMA

DELIVERABLES

- Verilog RTL source code
- Test bench with test suites
- Documentation including User's Guide and Integration Guide
- Technology-independent synthesis constraints

AXI PERFORMANCE SUBSYSTEM – ARM CORTEX A5



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