AHB Quad SPI Controller with Execute in Place (XIP)

DESCRIPTION

The Quad Serial Peripheral Interface module either controls a serial data link as a master, or reacts to a serial data link as a slave.

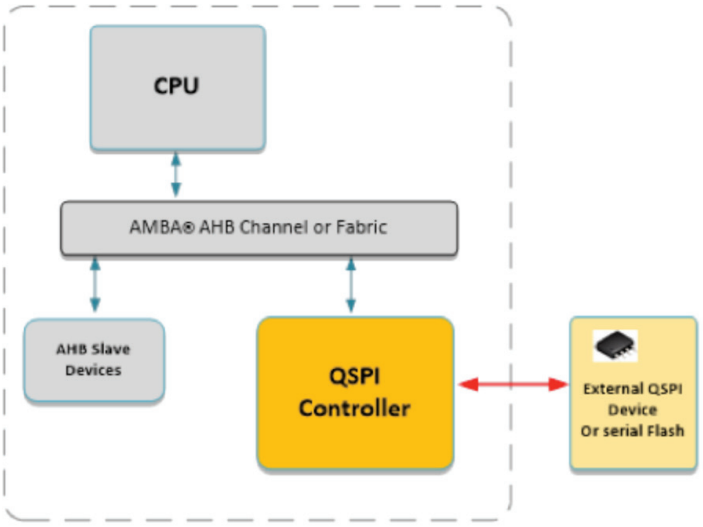
The IPC-QSPI-AHB bus controller can be configured under software control to be a master or slave device. Reading and writing the core is done on the AMBA AHB bus interface. The core operates in various data modes from 4 bits to 32 bits (8 modes are supported in multiples of 4 data bits). The data is then serialized and then transmitted, either LSB or MSB first, using the standard 4-wire SPI bus interface or the extended Quad mode bus.

AHB QUAD SPI CONTROLLER [XIP] IP CORE FEATURES

- 4 bit to 32 bit serial transmit & receive
- Full and half duplex modes
- Software programmable Master or Slave mode
- Software programmable SCLK rate for Master mode
- Quad-bit mode operation
- Dual-bit mode operation
- 64 word Tx and Rx FIFOs
- Asynchronous Slave Interface
- AMBA AHB interface
- Interrupt control
- LSB or MSB mode
- Up to 4 slaves under Master control
- DMA Interface
- Compatible with many industry-standard FLASH devices
- Execute-in-place (XIP) functionality for industry-standard FLASH devices

AHB QUAD SPI CONTROLLER [XIP] IP CORE DELIVERABLES

- Verilog Source
- Complete Test Environment
- AHB Bus Functional Model
- C-Sample Code



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