AHB-Lite to SPI Slave Bridge

DESCRIPTION

The AHB-Lite to SPI Slave Bridge IP core is commonly used as a monitor interface to allow external devices to access the internal AHB bus.

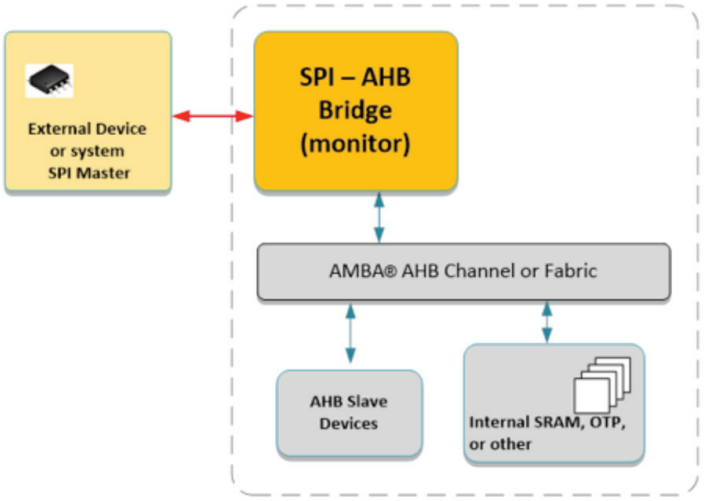
A SPI Slave to AHB-Lite Interface block provides read/write access by an external SPI device to the various memories and registers that are present in the chip's internal AHB-Lite subsystem. The Bridge converts SPI transactions into AHB Read or Write instructions, allowing the external SPI device to have full access to all memory mapped devices present in the AHB-Lite subsystem.

The SPI protocol layer is responsible for several things including:

- Interpreting commands from the low-level SPI interface (R/W, address, mode, protection, burst length)
- Generating an AHB Read or Write transaction based on the command received from the SPI interface
- Presenting (parallel) address and write data from the low-level SPI interface to the system
- Presenting (parallel) read data from the system to the low-level SPI interface

SPI SLAVE TO AHB LITE MASTER IP CORE DELIVERABLES

- Verilog Source
- Complete Test Environment
- AHB Bus Functional Model
- C-Sample Code



SPI SLAVE TO AHB LITE MASTER IP CORE FEATURES

- AMBA® AHB Monitor
- Allows external devices to access the internal AHB Bus
- AHB Master Read/Write capability
- Useful for updating device software from and external device
- Useful for reading internal memory mapped registers and memory

For more information, please contact us at ip@silvaco.com.

SILVACO

HEADQUARTERS
2811 Mission College Boulevard, 6th Floor
Santa Clara, CA 95054
Phone: 408-567-1000
Fax: 408-496-6080

CALIFORNIA	sales@silvaco.com 408-567-1000
MASSACHUSETTS	masales@silvaco.com 978-323-7901
TEXAS	txsales@silvaco.com 512-418-2929

JAPAN	jpsales@silvaco.com
EUROPE	eusales@silvaco.com
FRANCE	eusales@silvaco.com
KOREA	krsales@silvaco.com
TAIWAN	twsales@silvaco.com
SINGAPORE	sgsales@silvaco.com
CHINA	cnsales@silvaco.com

WWW.SILVACO.COM

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