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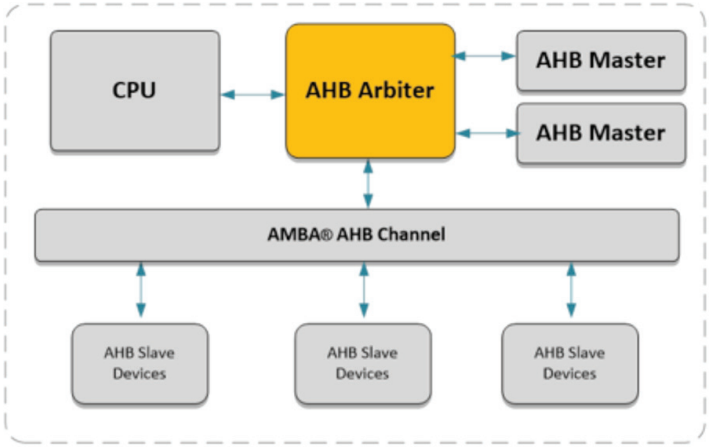
AHB Arbiter

DESCRIPTION

The AHB Arbiter arbitrates for the AHB bus among as many as four AHB masters. The AHB Arbiter implements a round-robin arbitration algorithm to AHB Masters that are requesting use of the bus. Only one master may control a given phase of the AHB transaction at a given time.

AHB is a pipelined bus in which there are three distinct phases: Arbitration Phase, Address (or Control) Phase, and Data Phase. A consequence of pipelining is that these phases overlap in time. For example, it is possible that Master A wins the Arbitration Phase that is coincident with the Address Phase owned by Master B and the Data Phase owned by Master C. It is in these terms that an AHB system must be discussed.

The AHB Arbiter has four distinct Mirrored-Master Ports, each of which can be connected to an AHB Master (e.g. a processor or a DMA Controller), and one Port that connects to an AHB subsystem, typically through an AHB Channel module.



AHB ARBITER IP CORE FEATURES

- AMBA® 2.0 Compatible
- Supports up to 4 AHB Masters
- Round Robin Arbitration
- Easily Expandable

AHB ARBITER IP CORE DELIVERABLES

- Verilog Source
- Complete Test Environment
- AHB Bus Functional Model
- C-Sample Code

For more information, please contact us at ip@silvaco.com.

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