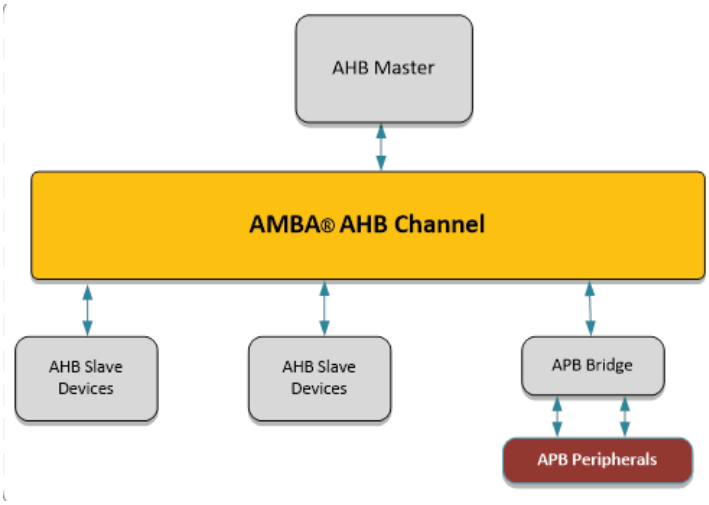
AHB Channel with Decoder and Data Mux IP Core

DESCRIPTION

The AHB Channel provides the necessary infrastructure to connect as many as 7 AHB Slaves (numbered 1-7) to an AHB bus Master. The AHB Channel performs a combinational decode on the incoming AHB address to produce the block selects for the various AHB Slaves. The address decoder contained in the AHB Channel has one area of memory reserved for a configurable remap application.

Typically, the AHB Channel is connected as in the following description. Each of the AHB Channel's 7 Mirrored Slave Ports is connected to an AHB Slave module (e.g. External Bus Interface, Memory Controller, AHB-to-APB Bridge.) On the Master side, the AHB Channel's Mirrored Master Port is connected either to an AHB Arbiter (in an AHB system with multiple bus Masters) or directly to an AHB Master such as a micro-processor (in an AHB system with a single bus Master.)



AHB CHANNEL IP CORE FEATURES

- AMBA® 2.0 Compatible
- Simple AHB Infrastructure for up to 7 AHB Slaves
- Multiple Masters can be easily accommodated using AHB Arbiter
- Includes Address Decoding
- Includes Read Data Muxing
- Remap to assist boot loading and debug

AHB CHANNEL IP CORE DELIVERABLES

- Verilog Source
- Complete Test Environment
- AHB Bus Functional Model
- C-Sample Code

For more information, please contact us at ip@silvaco.com.

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