AXI Quad SPI Controller with Execute in Place (XIP)

DESCRIPTION

The Quad Serial Peripheral Interface module either controls a serial data link as a master, or reacts to a serial data link as a slave.

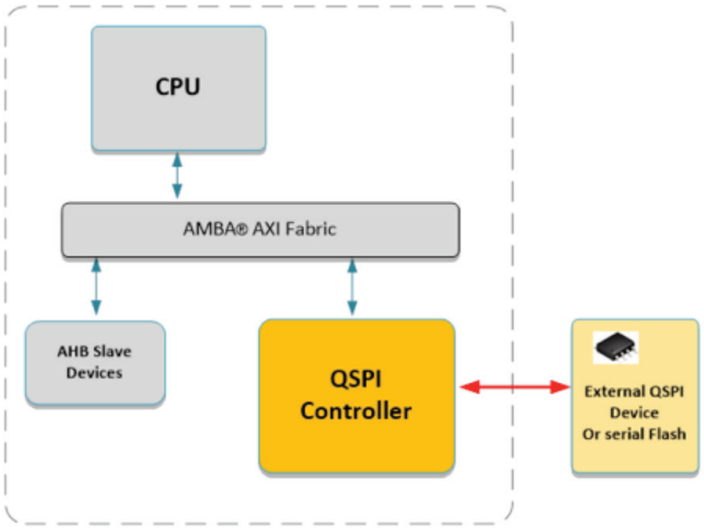
The IPC-QSPI-AXI bus controller can be configured under software control to be a master or slave device. Reading and writing the core is done on the AMBA AHB bus interface. The core operates in various data modes from 4-bits to 32-bits. The data is then serialized and then transmitted, either LSB or MSB first, using the standard 4-wire SPI bus interface or the extended Quad mode bus.

AXI QUAD SPI CONTROLLER [XIP] IP CORE FEATURES

- AMBA AXI interface
- Execute-in-place (XIP) functionality for several industry-standard FLASH devices
- DMA Interface
- Software programmable Master or Slave mode
- Software programmable SCLK rate for Master mode
- Quad and Dual-bit mode operation
- 4-bit to 32-bit serial transmit & receive – 1 bit increments
- Full and Half operation
- Separate SCLK input for Master Mode
- 8 to 256 word Transmit and Receive FIFOs - configurable
- Asynchronous Slave Interface
- Interrupt control
- LSB or MSB mode
- Up to 4 slaves under Master control

AHB QUAD SPI CONTROLLER [XIP] IP CORE DELIVERABLES

- Verilog Source
- Complete Test Environment
- AXI Bus Functional Model
- C-Sample Code



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