

HCS08 Processor

The HCS08 IP from Silvaco is the same 8-bit HCS08 microcontroller core implemented in NXP MC9S08xx family devices. Building on decades of leadership in the 8-bit microcontroller domain, the HCS08 extends the popular 68HC08 architecture, offering improved debug support and additional addressing modes to improve C code efficiency.

The HCS08 also provides a migration path to the 32-bit ColdFire® architectures. HCS08 and V1 ColdFire use the same single-pin debug interface and share a common set of development tools. With NXP CodeWarrior integrated development environment, assembly code for the HCS08 can be retargeted to the V1 ColdFire processor with just a few mouse clicks.

FEATURES

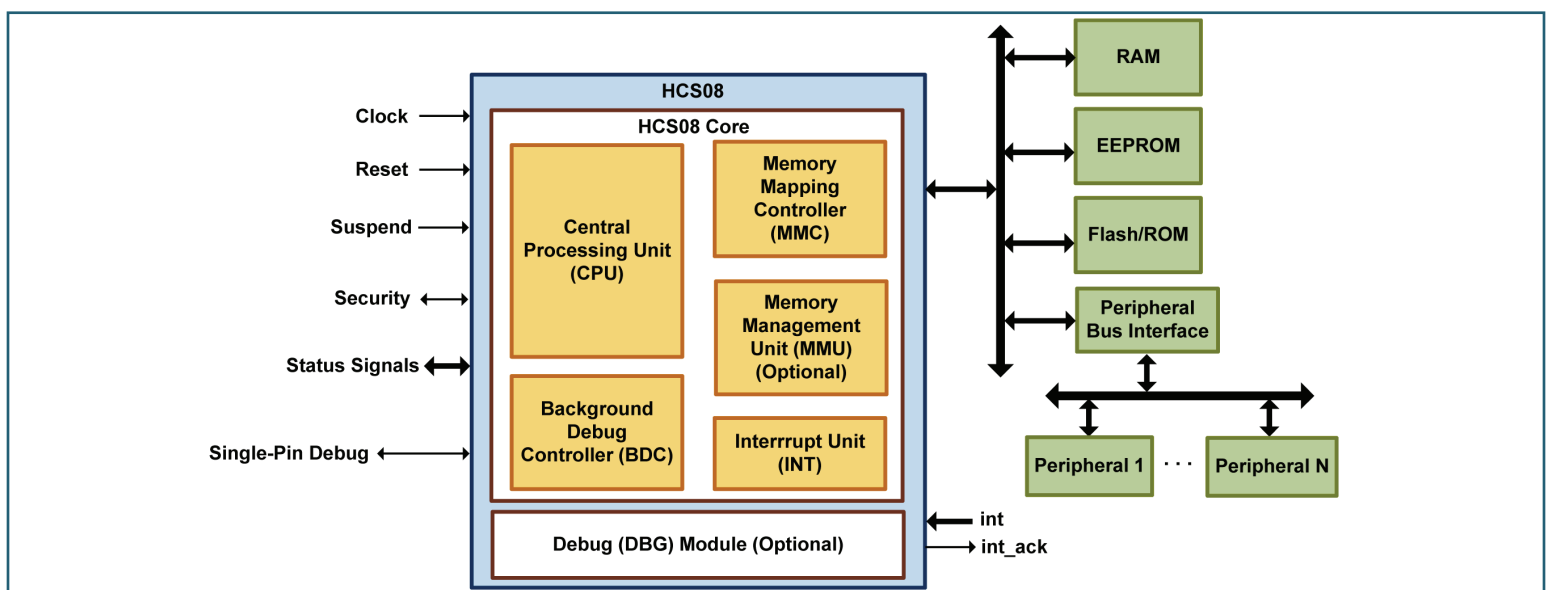
- 8-bit processor core with 16 or 17-bit address bus, depending on memory configuration
- 64-KB accessible program/data memory space (extended to up to 128 KB by an optional integrated Memory Management Unit (MMU))
- 68HC08 instruction set with added BGND instruction
- Additional addressing modes for the LDHX, STHX, and CPHX instructions improve C code efficiency
- 48 vectors for interrupt and reset sources
- Low-power mode support through the execution of the STOP and WAIT instructions
- Illegal address detection and management

- Security management
- Suspend mode to support initialization of memories before executing the first instruction
- Debug support through Background Debug Controller (BDC) module with single-wire interface to debug host
- Optional Debug (DBG) module for on-chip trace and enhanced breakpoint capabilities
- Fully-synthesizable, synchronous design
- Functional I/O signals registered at the core boundary

CONFIGURABLE MEMORY MAP

You can configure the HCS08 memory map to match any of 47 popular NXP HCS08-based devices. The configuration that you select determines the address ranges assigned to RAM, EEPROM, flash/ROM, Direct Page registers, and High Page registers. The configuration that you select also determines whether or not the MMU and DBG module are included. For example, if you select the MC9S08DZ128 configuration, the HCS08 includes the MMU and can address up to 128 KB (17-bit address bus), using both memory paging and linear addressing.

The MC9S08DZ128 configuration also includes the DBG module. For devices that include the DBG module, you can choose to remove the DBG module from your HCS08 IP configuration. For example, you can include the DBG module for prototyping and software development, then exclude the DBG module from your production devices.



DEBUG SUPPORT

An integrated BDC module provides sophisticated, non-intrusive software debugging and in-circuit programming of non-volatile memory. BDC features include:

- Single-wire interface to host development system
- SYNC command to determine communication rate
- BDC registers not located in memory map
- Background Debug Mode (BDM) out of reset
- BGND instruction or BACKGROUND command to enter BDM
- Foreground commands for memory access
- Background commands for CPU register access
- GO, GO_UNTIL, and TRACE1 commands
- One hardware address breakpoint built into BDC
- BACKGROUND command can wake CPU from WAIT or STOP mode
- Hardware handshake protocol to increase the performance of the serial communication
- Self-clocked interface for reliable serial communication using either CPU clock or dedicated (asynchronous) debug clock
- Debug clock can be disabled when BDC is not in use
- Special secure operation mode

The optional DBG module provides enhanced debug capabilities including:

- On-chip trace support using integrated FIFO with flexible triggering capabilities
- Address/data comparators generating FIFO triggers and/or breakpoints

DELIVERABLES

- Integration testbench and tests
- Documentation
- Scripts for simulation and synthesis with support for common EDA tools

For more information, please contact us at ip@silvaco.com.

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