

## ColdFire® V4 Core & SPP C1

The ColdFire V4 Core & Standard Product Platform (SPP) C1 (CFV4SPPC1) combines the ColdFire V4 Core with industry-proven platform peripherals to form a complete high-performance microcontroller subsystem supported by a vast ecosystem of development tools and runtime software. With the CFV4SPPC1, you get:

- Reliability—from processor and peripheral IP already deployed in millions of embedded systems worldwide
- Rapid time-to-market—in just a few hours you can be developing software on your own FPGA implementation of the CFV4SPPC1

### COLDFIRE V4 PERFORMANCE

The ColdFire V4 Core is a high-performance implementation of the ColdFire architecture with fast instruction throughput and high-speed Harvard local buses with tightly-coupled instruction and data caches and local SRAM. The ColdFire V4 Core also features an MMU for full operating system support plus special arithmetic hardware including a divider and enhanced MAC (EMAC) for faster execution of DSP algorithms, and an FPU for single and double-precision floating-point calculations.

Like all ColdFire architecture processors, the ColdFire V4 Core features a variable-length instruction set for maximum code density, industry-standard AMBA 2 AHB system bus interface for rapid system integration, and a wide selection of development tools, operating systems, drivers, and libraries from both commercial and open source providers.

### STANDARD PERIPHERALS AND INTERCONNECT

The CFV4SPPC1 includes ColdFire V4 Core, plus the fully-integrated peripherals shown in Figure 1, implementing functions commonly needed for embedded systems including interrupt control, DMA, timers, and various serial interfaces. An AMBA 2 AHB Crossbar Switch provides the system interconnect, supporting simultaneous AHB transfers between multiple masters and slaves, including externally-connected AHB masters and slaves.

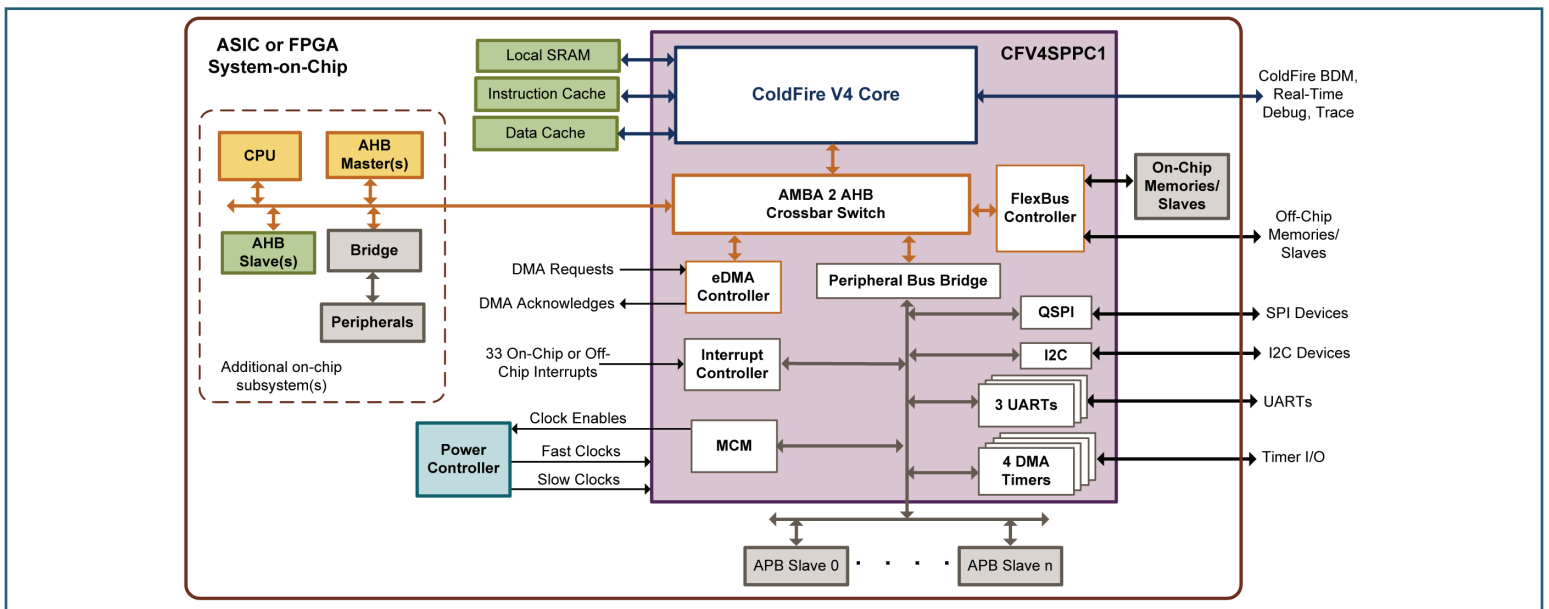
Variations of the CFV4SPPC1 with different combinations of on-board peripherals are also available.

### PERIPHERALS FEATURES

On-board peripherals and their features include:

- FlexBus Controller
  - Connects up to 6 on-chip or off-chip memories/devices
  - Independently programmable transfer characteristics for each device (wait states, address setup/hold)
- Enhanced DMA (eDMA) Controller
  - 16 independently programmable DMA channels
  - Programmable channel arbitration modes
  - Support for channel linking and scatter/gather operation

Figure 1. Example SoC Using CFV4SPPC1.



- Interrupt Controller
  - 64 programmable interrupt sources, 33 of which are available for external interrupts
  - Unique vector for each interrupt source
  - Support for low-power mode wake-up
- Queued SPI (QSPI) module
  - Programmable queue for up to 16 SPI transfers
  - Four chip-select lines for up to 16 devices
  - Programmable baud rate, before-and-after transfer delays, clock phase and polarity
- I2C interface module
  - Support for the original Philips I2C bus protocol
  - Support for baud rates up to 3.4 Mbps
- 3 UARTS
  - Programmable clock source, data formats, and modes (normal/loopback)
  - Error detection
  - Four maskable interrupt conditions
- 4 DMA Timer modules
  - Programmable clock source
  - Programmable prescaler
  - Programmable interrupt or DMA request upon timer event
- Miscellaneous Control Module (MCM)
  - Software watchdog timer
  - Reset status, low-power mode control, and core fault status registers

## POWER SAVING FEATURES

The CFV4SPPC1 features software-controlled shutdown of selected clocks to support a variety of chip-level low-power modes:

- Independent shutdown of selected peripheral clocks
- Shutdown of the ColdFire V4 Core CPU clock in response to a ColdFire STOP instruction; the ColdFire V4 Core local SRAM Controller clock may optionally be kept running in STOP mode to support access to local SRAM from external AHB masters

## DEBUG SUPPORT

The CFV4SPPC1 supports ColdFire Debug Architecture Revision D+, including:

- Background Debug Mode (BDM)
- Real-Time Trace (RTT)
- Real-Time Debug (RTD)
- On-chip, 128-entry trace buffer for low-cost trace over BDM

## DEVELOPMENT SUPPORT

The ColdFire architecture, including the ColdFire V2 Core, is supported by a vast assortment of development systems/tools and run-time software including libraries, stacks, drivers, and operating systems from providers such as NXP, Green Hills Software, Wind River Systems, and many more. A free version of the GNU compiler supporting ColdFire V2 targets is also available from [www.gnu.org](http://www.gnu.org).

NXP offers development boards, software, and CodeWarrior Development Tools (including a free version). In addition, there are several operating systems supporting the ColdFire V2 architecture, including uClinux and several RTOS's, such as the MQX RTOS from Embedded Access, Inc.

## DELIVERABLES

- Verilog source code
- Integration testbench and tests
- Documentation
- Scripts for simulation and synthesis with commonly-used EDA tools

For more information, please contact us at [ip@silvaco.com](mailto:ip@silvaco.com).

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