ColdFire V1 Platform

The ColdFire® V1 Platform (CFV1P) is a fully configurable microcontroller subsystem built from the same ColdFire V1 processor IP that is implemented in ColdFire+ family devices from Freescale Semiconductor. The ColdFire V1 Platform extends the core processor platform used in Freescale's MCF51Qx and MCF51Jx devices to include a set of production-proven peripheral modules, each of which can be included in or excluded from your ColdFire V1 Platform implementation depending on your system requirements.

PLATFROM FEATURES AND PERFORMANCE

The CFV1P features an enhanced version of the ColdFire V1 Core. Compared to the traditional ColdFire V1 Core used for the CFV1CORE product from Silvaco, the ColdFire V1 processor implemented in the ColdFire V1 Platform features:

- An enhanced MAC (EMAC) unit
- An improved hardware divider (DIV+)
- Cryptographic Acceleration Unit (CAU)

Each of the above units is optional. The ColdFire V1 debug unit with single-wire debug interface and 64-entry trace buffer is also optional. By adjusting HDL parameter settings, you can explore various design tradeoffs and include only the hardware you need for your final implementation, resulting in the smallest and most power efficient core possible for your application requirements.

Similar to other ColdFire architecture processors, the ColdFire V1 processor used in the ColdFire V1 Platform features a variable-length instruction set for maximum code density, industry-standard AMBA 3 AHB-Lite system bus interface for rapid system integration, and a wide selection of development tools, operating systems, drivers, and libraries from both commercial and open source providers.

STANDARD PERIPHERALS AND INTERCONNECT

The ColdFire V1 Platform also includes the fully-integrated peripherals shown in Figure 1, implementing functions commonly needed for embedded systems including interrupt control, DMA, GPIO, timers, and various serial interfaces. An AHB Crossbar Switch provides the system interconnect, supporting simultaneous AHB transfers between multiple masters and slaves, including externally-connected AHB masters and slaves.

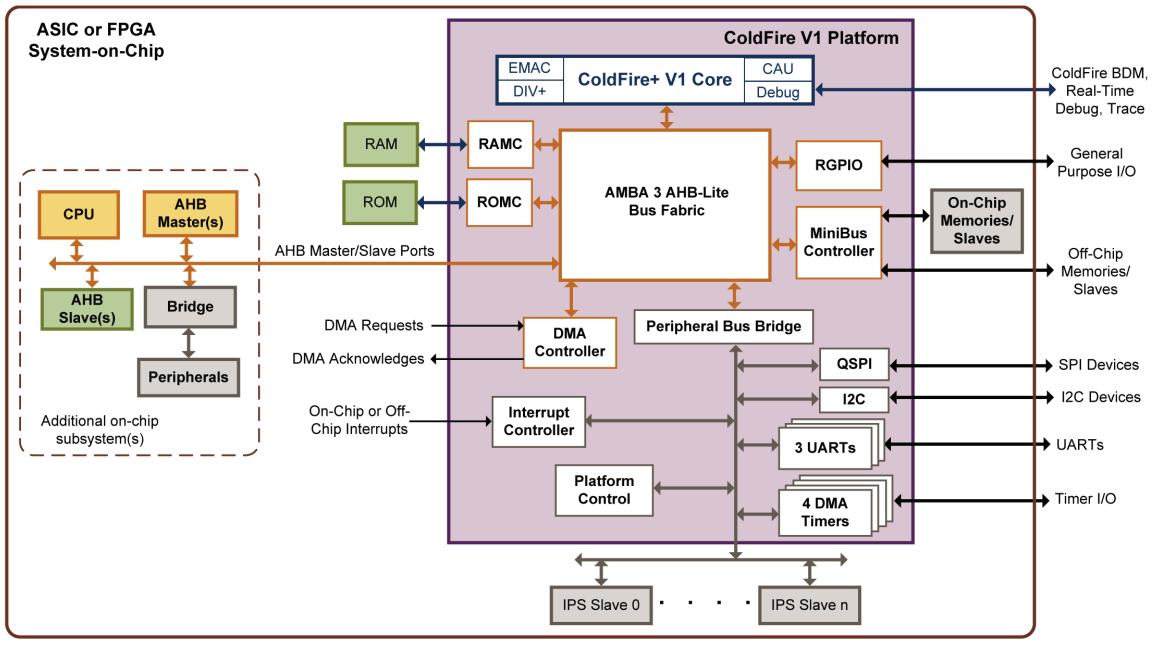
Most of the peripherals shown in Figure 1 are optional and can be configured in or out of your ColdFire V1 Platform implementation through HDL parameter settings.

PERIPHERALS FEATURES

On-board peripherals and their features include:

- RAM Controller (optional)
  - Supports tightly-coupled RAM with single-cycle access
  - RAM size can be 0, 2, 3, 4, 6, 8, 12, 16, 24, 32, 48, or 64 KB

Example SoC Using the ColdFire V1 Platform.



- ROM Controller (optional)
  - Supports tightly-coupled ROM with single-cycle access
  - ROM size can be 0, 4, 8, 16, 32, 64, 128, 256, 512, or 1024 KB
- MiniBus Controller (optional)
  - Connects one or two on-chip or off-chip memories/devices
  - Independently programmable transfer characteristics for each device (wait states, address setup/hold, data width, multiplexed or non-multiplexed mode)
- DMA Controller (optional)
  - Four independently programmable DMA channels
  - Sixteen possible peripheral DMA requests per channel
  - Support for channel linking
- Interrupt Controller
  - Supports 30 peripheral interrupt requests plus seven software interrupt requests
  - Unique vector for each interrupt source
  - Supports low-power mode wake-up
- Queued SPI (QSPI) module (optional)
  - Programmable queue for up to 16 SPI transfers
  - Four chip-select lines for up to 16 devices
  - Programmable baud rate, before-and-after transfer delays, clock phase and polarity
- I2C interface module (optional)
  - Support for the original Philips I2C bus protocol
- 0–3 UARTS (optional)
  - Programmable clock source, data formats, and modes (normal/loopback)
  - Error detection
  - Four maskable interrupt conditions
- 0–4 DMA Timer modules (optional)
  - Programmable clock source
  - Programmable prescaler
  - Programmable interrupt or DMA request upon timer event
- Platform Control
  - Software watchdog timer
  - Reset status, low-power mode control, and core fault status registers

POWER SAVING FEATURES

The ColdFire V1 Platform features software-controlled shutdown of selected clocks to support a variety of chip-level low-power modes:

- Independent shutdown of selected peripheral clocks
- Shutdown of the ColdFire V1 CPU clock in response to a ColdFire STOP instruction

DEBUG SUPPORT

The ColdFire V1 Platform supports ColdFire Debug Architecture Revision B+, including:

- Single-wire Background Debug Mode (BDM) interface
- Real-Time Debug (RTD)
- On-chip, 64-entry trace buffer for low-cost trace over BDM

DEVELOPMENT SUPPORT

The ColdFire architecture is supported by a vast assortment of development systems/tools and run-time software including libraries, stacks, drivers, and operating systems from providers such as NXP, Green Hills Software, Wind River Systems, and many more.

Freescale offers development boards, software, and CodeWarrior Development Studios (including a free version supporting ColdFire+ devices). In addition, there are several operating systems supporting NXP devices, including the MQX RTOS from Embedded Access, Inc.

DELIVERABLES

- Verilog source code
- Integration testbench and tests
- Documentation
- Scripts for simulation and synthesis with commonly-used EDA tools

For more information, please contact us at ip@silvaco.com.

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Rev 081919_03
70009