Hipex

Full-Chip Parasitic Extraction

SILVACO

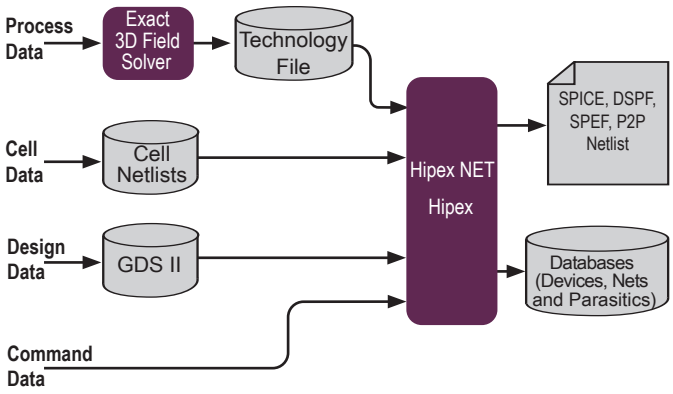
Hipex is an accurate and fast full-chip hierarchical extraction software that performs extraction of parasitic capacitances and resistances from hierarchical layouts. Hipex is tightly integrated with the Expert Layout Editor for complete design flow of DRC/LVS and RC parasitic extraction.

Key Features

- User-programmable netlist extraction provides custom set of extracted parameters (e.g. Well Proximity, STI stress effects)
- Multiple parasitic extraction models, including lumped RC, C only, R only, coupled C and fully distributed RC
- Selected net extraction for fast RC extraction of critical path nets in SoCs and large memories
- Efficient network reduction for distributed parasitic RC networks
- Output parasitic netlist files in SPICE, DSPF, SPEF, and P2P formats
- Automated back annotation enables accurate post-layout simulation and analysis
- Field solver mode provides accurate parasitic resistance/capacitance calculation
- Rapid rule-based approach consisting of using built-in and custom equations for parasitic extraction
- Different modes of parasitic extraction and their combinations provide various solutions in terms of trade-off between accuracy and productivity

Hipex NET Device Extraction

- Integrated into Expert Layout Editor
- Supports custom technologies (i.e. LCD, analog, mixed) and industry-standard PDKs
- Extracts hierarchical netlist preserving original layout hierarchy for easy analysis
- Extracts MOSFET, MESFET, BJT, JFET, diode, capacitor, resistor, and parameterized user-defined devices
- Performs electrical rule checking (ERC) for shorts, opens, dangles
- Provides full customization for a set of extracted parameters
- Accurate device extraction for non-45 and non-90 degrees devices
- Efficient memory usage for handling large designs
- Maintains netlist data base for back-annotation and device/net probing



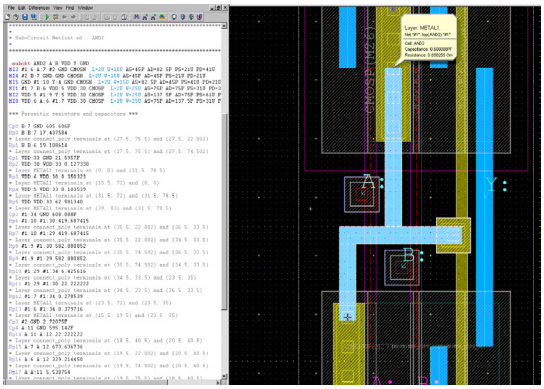
Hipex Full-Chip Parasitic Extractor Product Design Flow.

Hipex Parasitic Capacitance Extraction

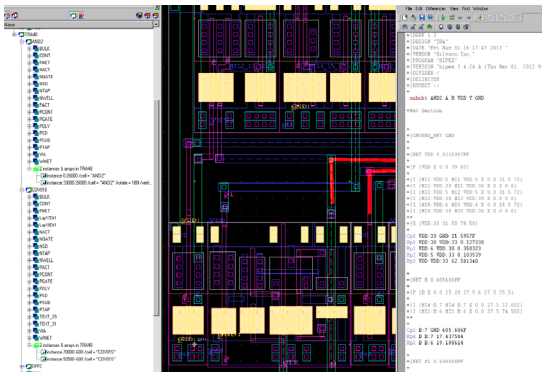
- Driven by rule-based technology file
- Offers Field Solvers based approach for very accurate parasitic capacitance extraction
- Back-annotates the schematic netlist with parasitic capacitors
- Striping algorithm and stripe database enables efficient parallelization for multi-processor machines
- Supports black-boxing for integration with routing tools
- Extracts parasitic coupling capacitors for full chip and selected nets
- Offers user-defined or built-in capacitance models
- Supports external capacitance rule files generated by Exact for 3D accurate mode
- Creates incremental capacitance database on a net-by-net basis
- Extracts selected nets for fast parasitic C computation of critical paths
- Offers non-shielded (multilateral) capacitance model for display designs
- Provides custom corner and overlap models for more accurate capacitance calculation

Hipex Parasitic Resistance Extraction

- Driven by rule-based technology file
- Back-annotates the schematic netlist with parasitic resistors
- Supports Distance/Width process deviations
- Processes L, T, Cross, and Bend resistor shapes
- Accepts user-defined scripts for custom computing of resistance
- Uses contact over-sizing and clustering to simplify resistor shapes
- Extracts netlist with parasitic resistors hierarchically for full chip or selected nodes
- Creates incremental resistance database on a net-by-net basis
- Multiple extraction models and equation solvers are used for arbitrary shape resistors
- Splits long conducting tracks for more accurate RC distribution
- Provides field-solver mode to obtain precise resistance for difficult areas (such as regions with numerous contacts and multi-layer buses)



Hipex RC database provides visualization of parasitic elements on Expert layout view.



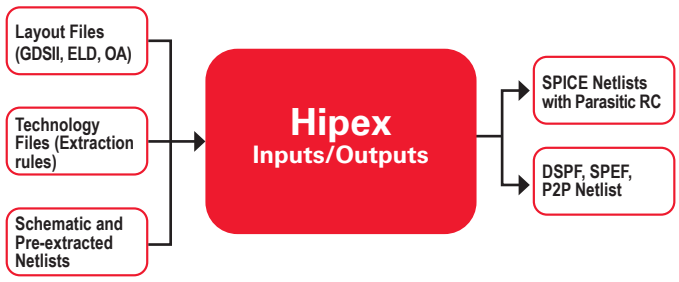
Hipex supports SPICE, DSPF, or SPEF formats.

Hipex Parasitic Network Distribution

- Combines extracted nodes with parasitic resistance and parasitic capacitance
- Distributes both coupling and ground capacitors
- User-defined threshold for minimum resistance and capacitance
- Distributes capacitors over parasitic resistor bodies accurately using stored locations
- Uses thrifty and detailed models for RC network
- Results are output to SPICE, DSPF, SPEF, P2P netlists
- Back-annotates extracted netlist with schematic node names
- Supports P2P format to present per net capacitance and point-to-point resistance

Hipex-CRC Network Reduction Tool

- Significantly reduces runtime of post-layout and post-route simulations
- Performs reduction using Time Domain and Scattering-Parameter-Based Macromodeling methods
- Eliminates dangling RC elements and elements bounded by user specified threshold; performs parallel/series merging
- Performs networks reduction in linear time
- Handles RC networks with loops
- Preserves the accuracy of simulation for reduced RC networks
- Supports SPICE, DSPF, or SPEF formats
- Custom reduction by variation of settings



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