Gateway

Schematic Editor

SILVACO

Gateway supports flat or hierarchical designs of any technology. Gateway readily accepts legacy designs from other schematic editors through OA and EDIF import.

Key Features

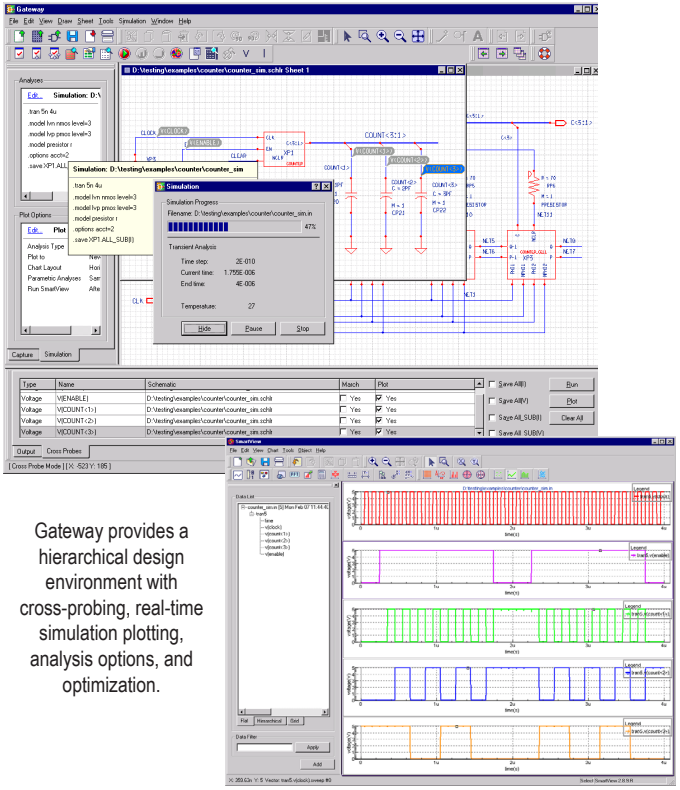
- Powerful schematic capture and editor functionality to create and modify multi-view, multi-sheet, hierarchical IC designs
- Seamless integration with SmartSpice Circuit Simulator that creates an interactive design environment with behavioral models, cross-probing, waveform display, and analysis
- Create HSPICE compatible input decks
- Creates Verilog (IEEE 1364) input decks and integrated with our digital simulator, Silos
- Controls multi-user projects with shared workspaces for libraries of cells and symbols used by the design team
- Creates netlists for a variety of uses including, simulation, LVS, NDL/SDL and CDL from one schematic
- Drives Expert layout editor connectivity and automatic placement
- Silvaco's strong encryption is available to protect valuable customer and third party intellectual property
- Advanced scripting support using Javascript

Ease of Use and Adoption

- Extensive set of PDKs
- Easy to use for both new and experienced designers with intuitive left-to-right design approach, tool tips, and batch simulation control
- Easy to set up multi-user environment with design libraries and import legacy data using EDIF
- Help functions and tool tips for new users
- Batch mode simulation options directly accessible from schematic
- Parameter minimum/maximum checking eliminates entry errors
- Supports wire to wire, wire to pin, wire by name, and implicit/global connections including industry standard Inherited Connections capabilities

Full Functionality

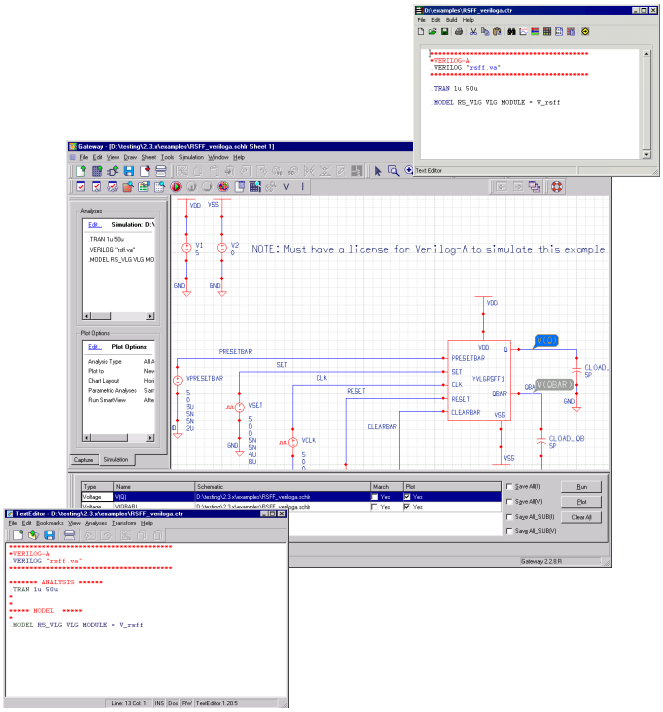
- Easy to create symbols, subcircuits, subschematics, and Verilog-A models
- Comprehensive symbol creation and editing features for simulation, schematic-driven-layout, and LVS compatibility
- User-configurable keys for repetitive tasks and to emulate legacy capture tools
- Hierarchical capture for modular, reusable designs, libraries, and working with legacy circuits
- Powerful edit-in place functions with wires, busses, bus ripping, and bus merging
- Designer configurable rule checks show electrical drawing rule violations and illegal names
- Gateway can use Verilog or SPICE netlists to create symbol files for use in designs



Gateway provides a hierarchical design environment with cross-probing, real-time simulation plotting, analysis options, and optimization.

Integrated Custom IC Design Platform

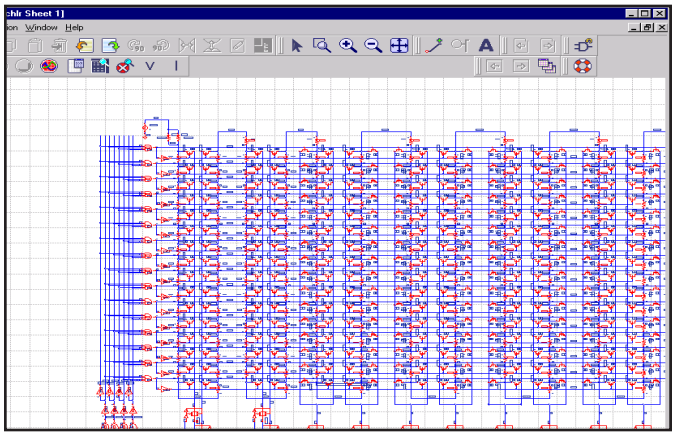
- Front-to-back design automation solution for custom analog circuits
- Silvaco behavioral modeling, schematic capture, circuit simulation, layout editing, DRC, LVS, and parasitic extraction are included in a proven design flow
- Integrated with SmartView waveform analyzer for overlaid measurements of delays, slopes, overshoots, rise-time, and eye diagrams – complete with vector calculator
- Powerful cross-probing between schematic and SmartView provide real-time design feed back
- Call-backs evaluate expressions in real-time for design rules, tolerances, parametric calculation, and process skews
- Annotation and display of device operating conditions including MOS operating region and DC bias voltages and currents, throughout the hierarchy



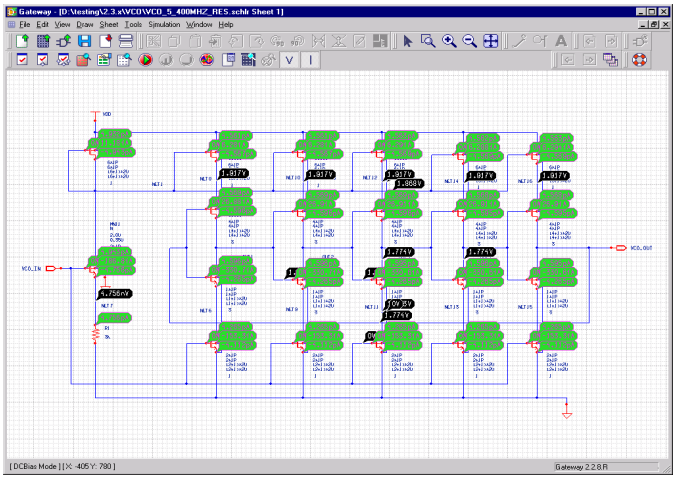
Gateway provides an environment for mixing transistor and behavioral level (Verilog-A) schematics to minimize design time and maximize efficiency. Verilog-A schematics may be used for behavioral block design or compact model design.

Designer Productivity

- Supports encrypted netlists behind symbols in design kits for IP distribution
- Real time incremental plotting of simulation results to monitor long simulations
- Efficient control of the design flow between schematic, simulation, and analysis
- Highlights errors and zooms to schematic location/level for correction



Gateway applications include interactive IC design to build and port digital and analog blocks, standard cells, I/OS, and, as shown above, hierarchical memories.



DC bias for currents and voltages for hierarchical and flat drawings.

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Rev 040920_13