

Utmost IV

Device Characterization and SPICE Modeling

SILVACO

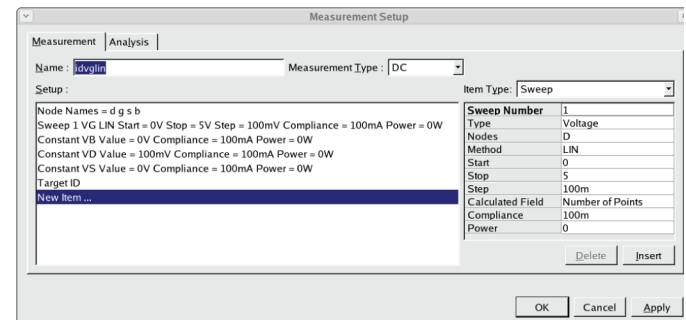
Building on many years' experience, Utmost IV provides a powerful yet easy-to-use tool for the characterization of devices and the generation of accurate, compact models, macro-models, and Verilog-A models for analog and RF applications.

Key Features

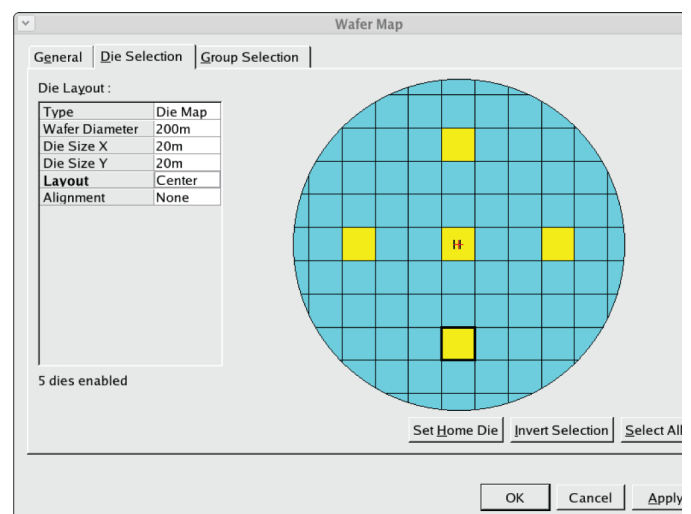
- Automated measurement and SPICE model extraction of any device type
- Full control of all measurement conditions with over 100 different measurement instruments supported
- Open architecture instrument drivers can be modified or created by user
- Extract any compact, macro-model or Verilog-A SPICE model
- Combine direct extraction and parameter optimization techniques
- Simulate and optimize any combination of data including extracted data values
- Family of advanced optimizers, including genetic type optimizers
- High-speed multi-threaded SmartSpice interface
- Supports SmartSpice, HSPICE, Eldo and Spectre simulators
- Verilog-A model and extraction sequence co-development platform
- Integration with TCAD tools provides process simulation to SPICE model development flow
- Store your data in either the file system or in a database
- Store, share and re-use data using optional Firebird relational database
- Easy data import from Utmost III legacy data, TCAD simulation files or third party data files

Measuring Devices in the Acquisition Module

- Supports all types of semiconductor devices
- Perform any measurement and control all measurement conditions
- Variables can be used within measurement setups to increase re-usability
- Embed extractions in measurement sequence so that extracted result from one measurement can be fed into the conditions of another measurement
- Supports over 100 measurement instruments
- Open interface allows user to create new or modify existing instrument drivers
- Data can also be generated from simulation, which is useful when converting one model type to another



Flexible, easy-to-use interface can define any measurement.



Fully automated sequence of measurements.

Supported Measurement Instruments Include

DC Instruments

agilent_b1500
agilent_b1505
agilent_e5260
agilent_e5270
agilent_hp_4155a
agilent_hp_4155b
agilent_hp_4155c
agilent_hp_4156a
agilent_hp_4156b
agilent_hp_4156c
hp_4141
hp_4142
hp_4145
keithley_4200
keysight_b1500
keysight_b1505
keysight_e5260
keysight_e5270
tektronic_370
tektronic_371

LCR (Capacitance) Instruments

agilent_b1500
agilent_b1505
agilent_e4980
hp_4274
hp_4275
hp_4276
hp_4277
hp_4279
hp_4280
hp_4284
hp_4285
hp_4294

LCR (Capacitance) Instruments (con't)

keithley_590
keithley_595
keysight_b1500
keysight_b1505
quadtech_7600

AC (s-parameter) Instruments

agilent_ena
agilent_pna
anritsu_37xxxD
hp_8510c
hp_8719d
hp_8719es
hp_8720d
hp_8720es
hp_8722d
hp_8722es
hp_8753a
hp_8753b
hp_8753c
hp_8753d
hp_8753e
hp_8753es
keysight_ena
keysight_pna
rohde_schwarz_znb

Scanners

agilent_b2200
agilent_b2201
agilent_hp_e5250

Scanners (con't)

hp_3235
hp_3488
hp_3495
hp_3852
hp_4084
hp_4085
hp_4086
keithley_7001
keithley_7002
keithley_705
keithley_706
keithley_707
keithley_708
keysight_b2200
keysight_b2201
keysight_e5250

Probers

alessi_rel2500
alessi_rel4500
alessi_rel5500
alessi_rel6171
cascade_summit_11500
cascade_summit_12000
electroglas_1034
electroglas_2001
electroglas_4080
electroglas_commander
karl_suss_pa200
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Probers (con't)

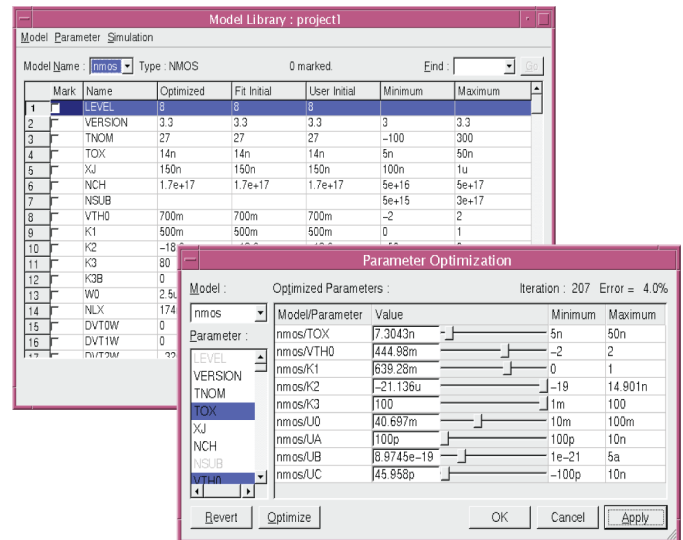
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wentworth_us

Thermal Controllers

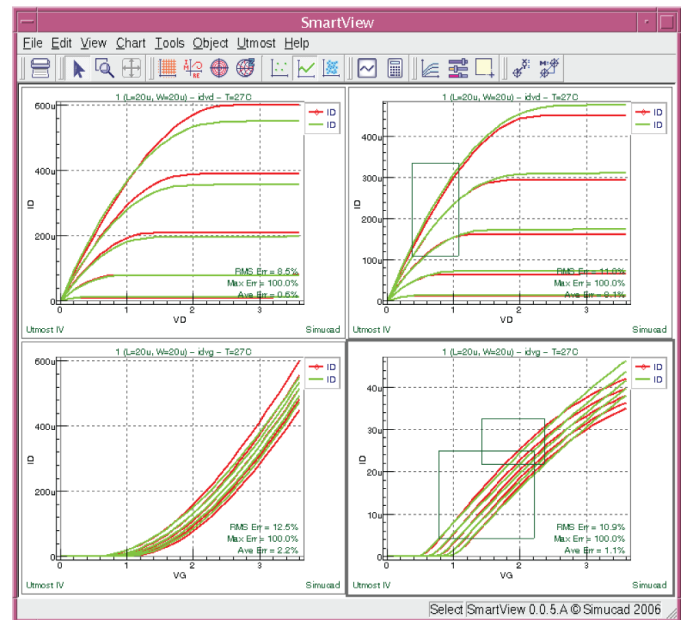
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delta_9010
delta_9388
electroglas_tc2000
ers_sp53
ers_sp62
etac_fx4050
micronics_wec10
ransco_900
temptronic_tp03000
temptronic_tp03100
temptronic_tp04100
tenney_junior
thermonics_t2420
thermonics_t2500
thermonics_t2600
thermonics_t2820
thermotron
triotech_tc1000
triotech_tc2800

Generating SPICE models in the Optimization Module

- SPICE model generation using any combination of direct parameter extraction or parameter optimization
- Supports all technologies
- Supports compact, macro-model or Verilog-A model extraction
- High-speed interface to SmartSpice simulator performs hundreds of simulations per second
- No simulation slowdown when using macro-models
- Selection of any combination of data targets to perform optimization
- Extract and display any device figure of merit, such as threshold voltage
- Plot, simulate and optimize device figures of merit
- Optimization sequence provides fully automated SPICE model generation mode
- Interactive rubberband sliders instantly show the effect of changing model parameters on the simulated characteristics
- Family of advanced local and global optimizers include:
 - Levenberg-Marquardt
 - Hooke-Jeeves
 - Genetic Optimizer
 - Simulated Annealing
 - Parallel Tempering
 - Differential Evolution
- Hybrid optimization combines the power of the global optimizer with the speed of the local optimizer
- Define model parameters as values or as expressions
- Directly import models from hierarchical SPICE library files, including parameters defined as expressions
- Import and simulate process corner or other complex model formats
- Perform simulations using external model libraries



Rubberband optimization of any number of parameters.



View and optimize any number of targets.

Corner and Retargeting Module

- Creating corner models or retargeting existing models
- Quick model tuning using electrical test (ET) data tables and trend plots
- Flexible target and measurement setup definitions
- Fast simulation engine

Quick-Start Optimization Project Templates

- Help users create optimization projects for their data
- Easy project configuration based on templates
- Quickly achieve accurate model cards
- Experienced users can tweak the project more

Developing Verilog-A Models and Extraction Strategies

- Utmost IV is the perfect Verilog-A model development tool
- Modify Verilog-A model code and instantly see effect on simulated characteristics
- Use data from any source including measurement, TCAD process simulation or other SPICE model simulation to develop new Verilog-A model code and parameters
- Interactive rubberband sliders allow parameter limits to be quickly explored
- Compare model versions
- Side-by-side development of the Verilog-A model and the extraction strategy for the model

Using TCAD Simulations to Generate SPICE Models

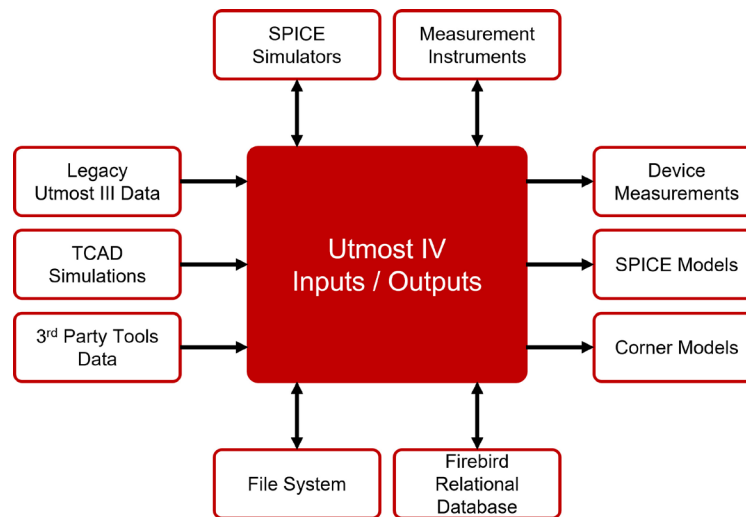
- Full TCAD process simulation to SPICE model generation flow
- Provide 'level 0' SPICE models to designers even before the process is available
- Compare TCAD simulations with measured data from the process
- Combine TCAD and measured data to develop SPICE models
- Seamless integration with DeckBuild and VWF tools

Optional Relational Database Organizes Your Work

- As well as normal file storage, Utmost IV offers a relational database to store your measurement data and projects
- Avoids storage and duplication of thousands of separate data files in difficult to locate file systems
- Provide controlled access to information with full user and group permission settings
- Facilitates sharing and easy retrieval of data
- Database is proven Borland Firebird relational database

Custom Automation Using Script Mode

- Combine the power of Utmost IV with the customization capability of JavaScript programming language
- Perform any measurement, simulation, extraction, or optimization
- Access any database or file
- Export a script version of any Acquisition or Optimization project for rapid script development



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