I3C V1.1 Advanced Family for Sensor and IoT Applications

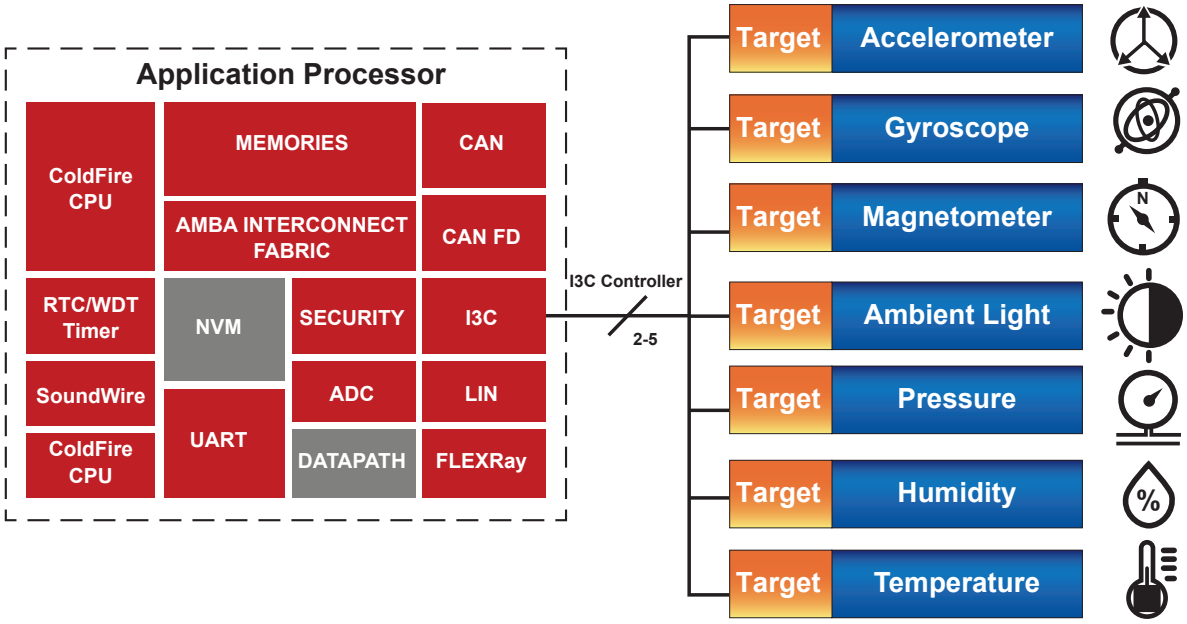
SILVACO

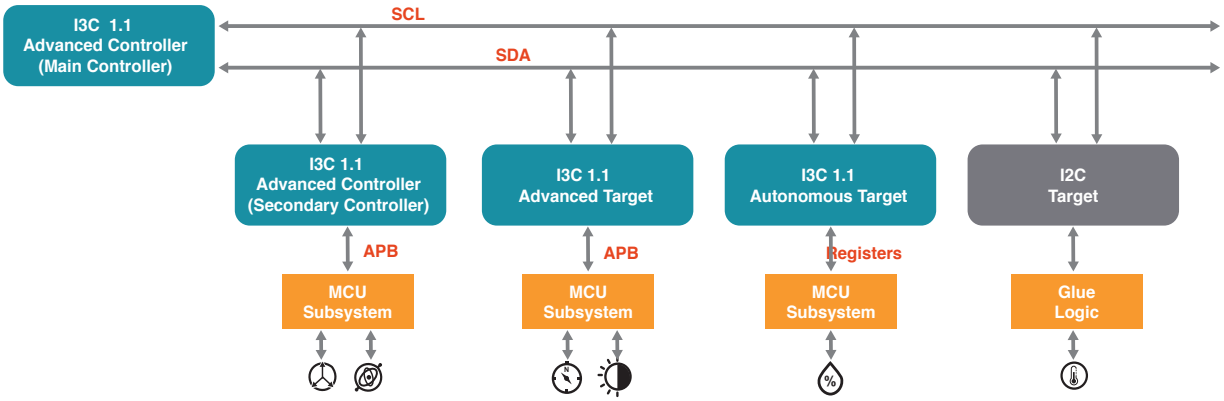
Overview

I3C is a new a standard from the MIPI Alliance that unifies and extends the legacy interfaces of I2C and SPI and adds new powerful features to support modern mobile, automotive, and IOT applications. The range of I3C products from Silvaco allows customers to take full advantage of the high performance and low power features of I3C V1.1.

Applications

- Mechanical sensing (Gyroscopes, MEMS, etc.)
- Environmental sensing (Light, pressure, temperature, humidity, etc.)
- Biometrics (Fingerprinting, glucose, heart rate, breathalyzer, etc.)
- Communication (Near-field sensors, infrared remotes, etc.)





Sensor Connections

I3C 1.1 Advanced Controller

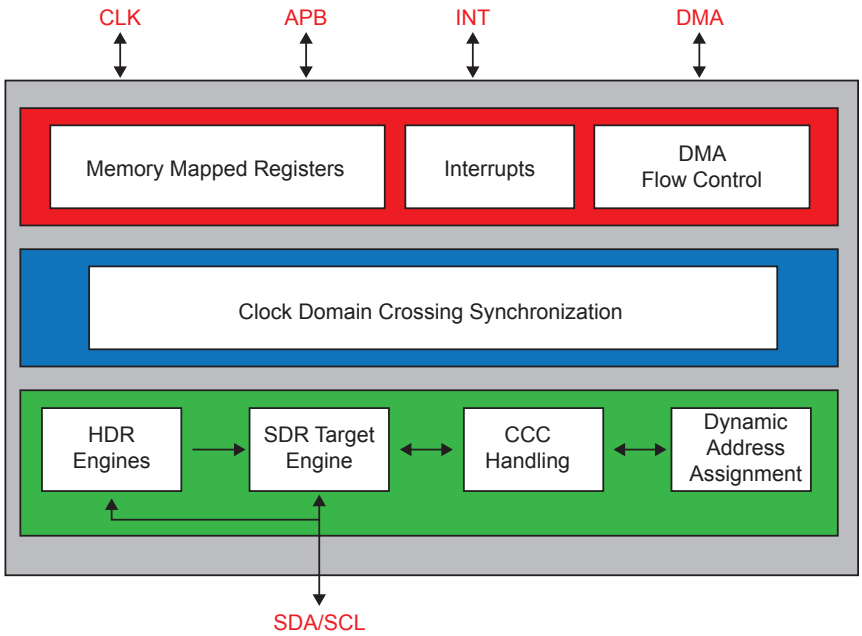
Overview

The I3C Advanced Controller is a highly configurable I3C controller that can be used in microcontroller-based environments to provide I3C connectivity to any device. It contains controller capabilities as well as many of the same features as the I3C Advanced Target. It can be configured in a number of different ways to allow the core to use the minimum amount of logic to reduce both area (cost) and power.

Features

- Highly configurable core that allows customer to minimize unneeded logic
- Compliant with MIPI I3C V1.1.1
- Compliant with MIPI I3C Basic V1.1.1
- Dynamic addressing
- Single Data Rate (SDR)
- Error detection types (TE0-TE5, CE0, CE2, CE3)
- Advanced I3C features
  - HDR-BT with up to 100 Mbps bandwidth
  - Multilane with 1, 2, or 4 SDA lanes
  - Hot-join
  - In-band interrupts
  - Timing Control
    - Asynchronous Mode 0
    - Synchronous Mode
  - High-speed mode (HDR-DDR)
  - Group addressing
  - Target reset
  - All Common Command Codes (CCCs) supported
- AMBA APB (v3) application interface
  - Memory mapped registers
  - DMA, flow control features
  - FIFO options
    - Internal 2-byte ping-pong buffer
    - Internal FIFO (or 32 words for HDR-BT mode)
- Legacy I2C coexistence, including I2C messaging
- Static I2C address support
- Support for I2C pads with 50ns glitch filter

Block Diagram



I3C 1.1 Autonomous Target

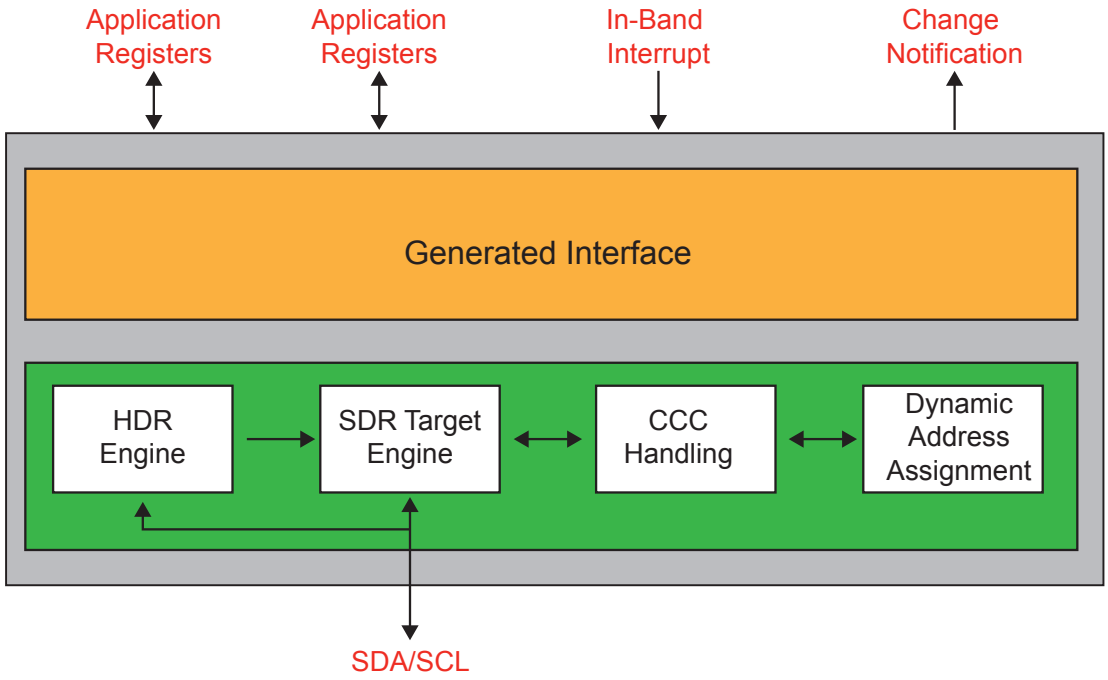
Overview

The I3C Autonomous Target is intended for simple, data acquisition types of applications where a microprocessor is not needed to process the data. Instead, data is exchanged via a simple set of register interfaces to the application and the controller autonomously manages all of the communication to an upstream I3C Controller.

Cache Types

- Highly configurable core that allows customer to minimize unneeded logic
- Compliant with MIPI I3C V1.1.1
- Compliant with MIPI I3C Basic V1.1.1
- Dynamic addressing
- Single Data Rate (SDR)
- Error detection types (TE0-TE5)
- Advanced I3C features
  - Hot join
  - In-band interrupts
  - Timing Control
    - Asynchronous Mode 0
    - Synchronous Mode
  - High-speed mode (HDR-DDR)
  - Group addressing
  - Target reset
  - All Common Command Codes (CCCs) supported
- Static I2C address support
- Legacy I2C coexistence, including I2C messaging
- Support for I2C pads with 50ns glitch filter

Block Diagram



I3C 1.1 Advanced Target

Overview

The I3C Advanced Target is a highly configurable I3C Target that can be used in microcontroller based environments to provide I3C connectivity to any device. It can be configured in a number of different ways to allow the core to use the minimum amount of logic to reduce both area (cost) and power.

Cache Types

- Highly configurable core that allows customer to minimize unneeded logic
- Compliant with MIPI I3C V1.1.1
- Compliant with MIPI I3C Basic V1.1.1
- Dynamic addressing
- Single Data Rate (SDR)
- Error detection types (TE0-TE5)
- Advanced I3C features
  - HDR-BT with up to 100 Mbps bandwidth
  - Multilane with 1, 2, or 4 SDA lanes
  - Hot join
  - In-band interrupts
  - Timing Control
    - Asynchronous Mode 0
    - Synchronous Mode
  - High-speed mode (HDR-DDR)
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  - All Common Command Codes (CCCs) supported
- AMBA APB (v3) application interface
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Block Diagram